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Tunneling Transistors for Low Power Electronics

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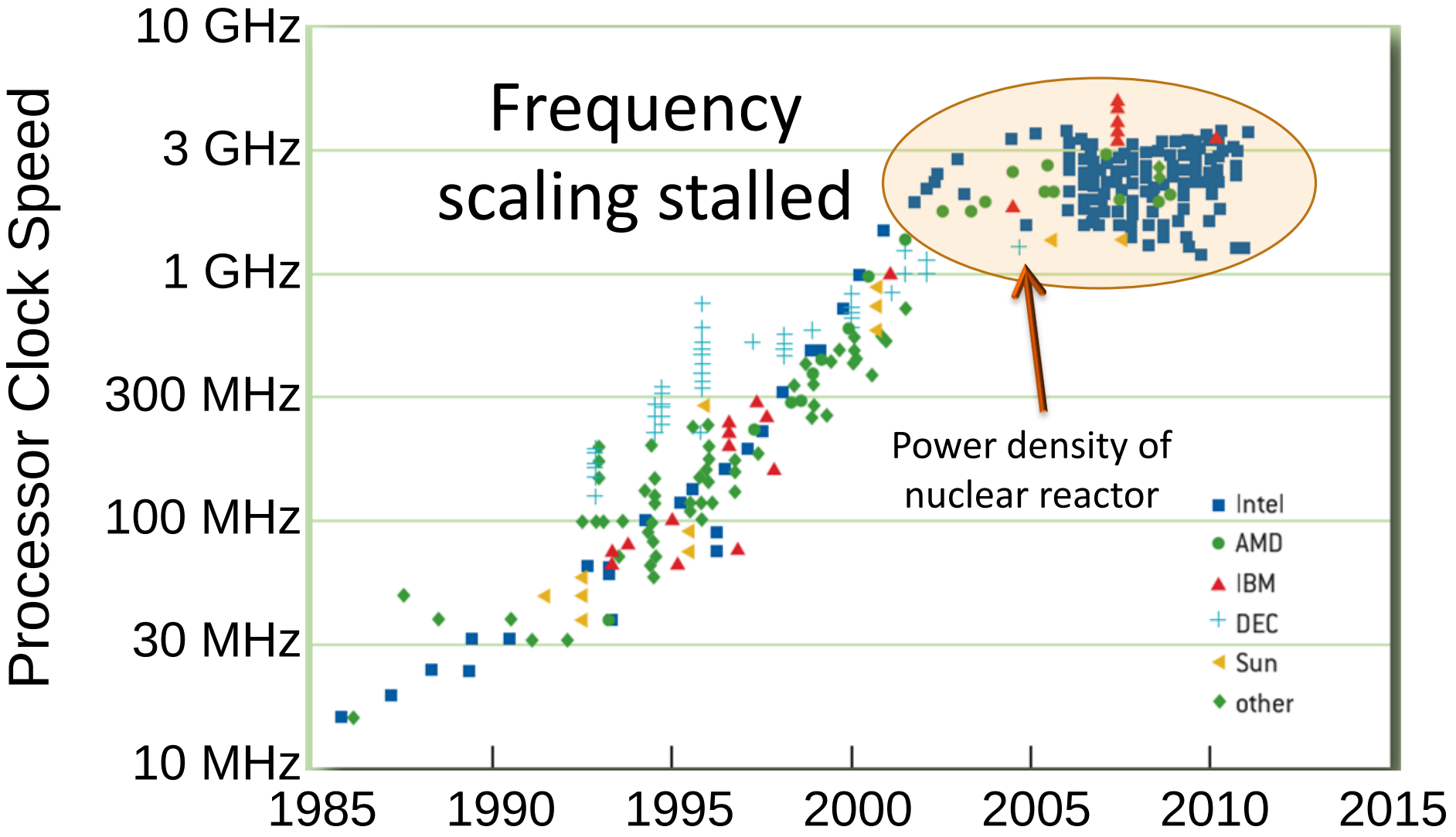
Support from NSF E3S Center

MOSFET

TFET

(tunneling transistor)

MOSFET Scaling Crisis



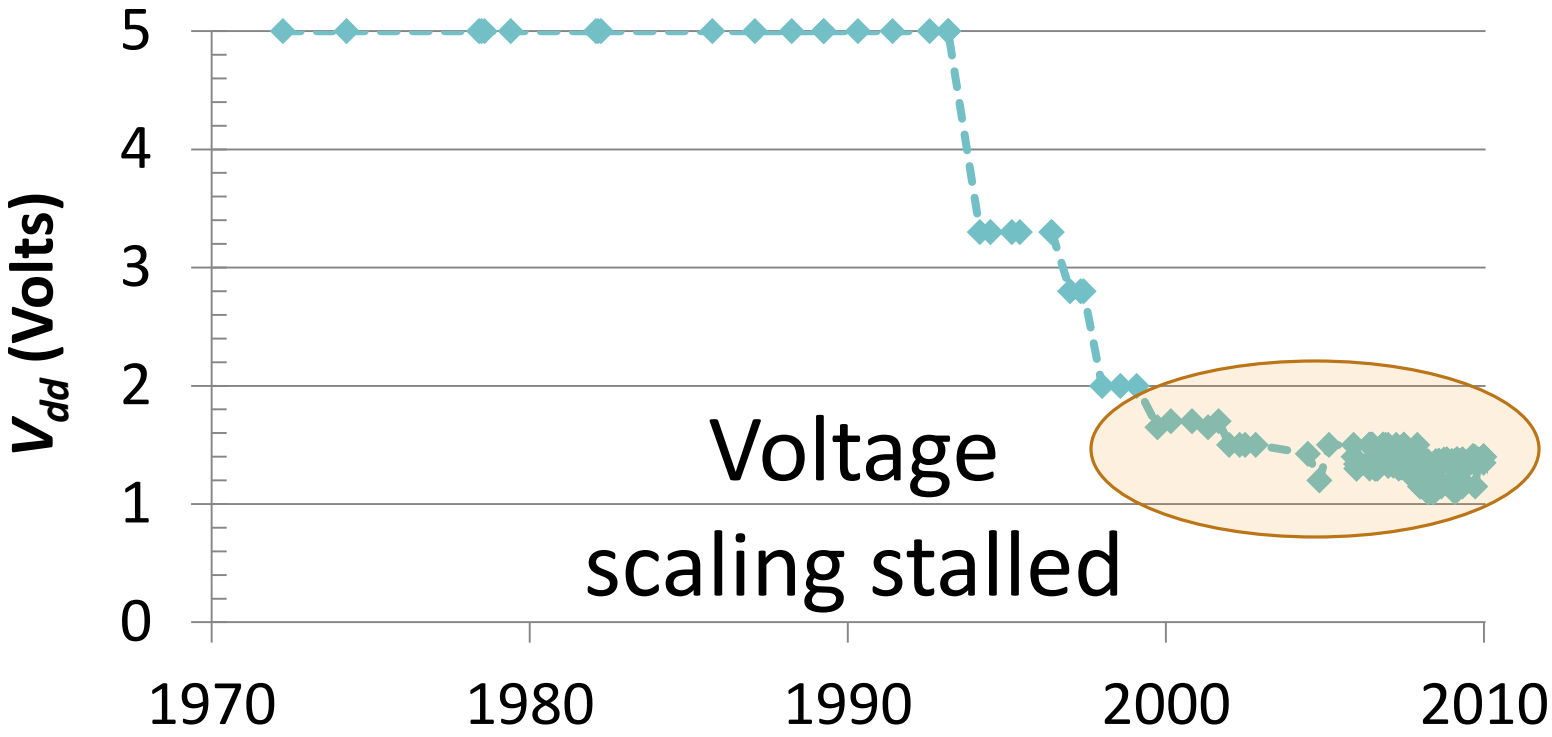
A. Danowitz, K. Kelley, J. Mao, J. P. Stevenson, and M. Horowitz, "CPU DB: Recording Microprocessor History," *Queue*, vol. 10, no. 4, pp. 10:10–10:27, 4/2012.

Power & Voltage Scaling

$$P_{active} = \alpha C V_{dd}^2 f$$

$$P_{passive} = I_{off} V_{dd} + I_G V_{dd}$$

$$P_{total} = P_{active} + P_{passive}$$



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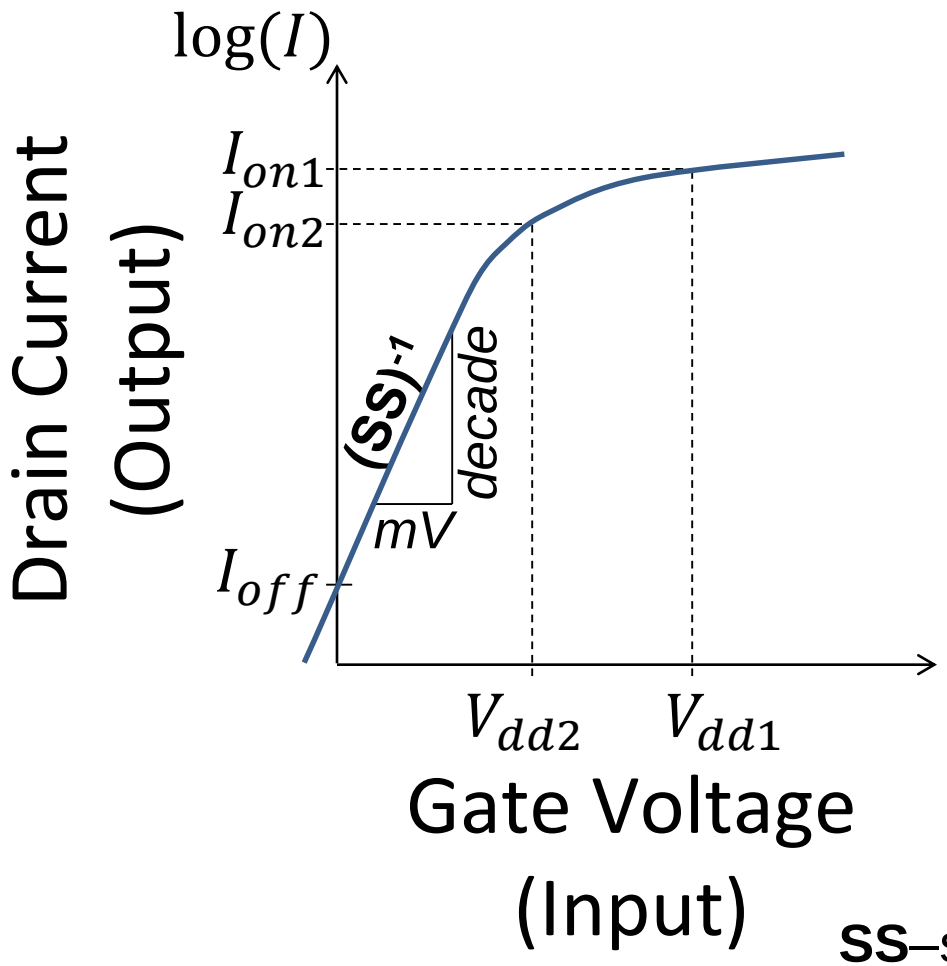
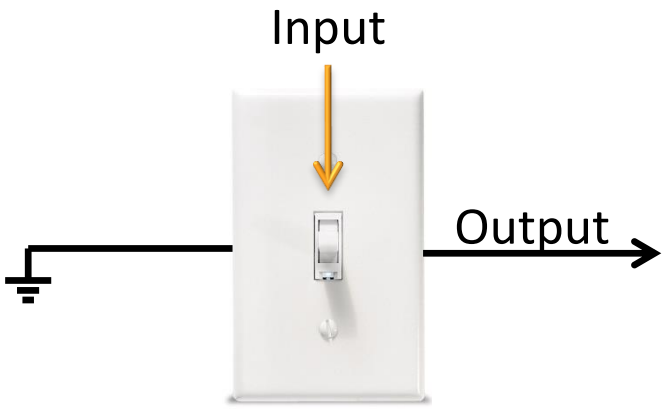
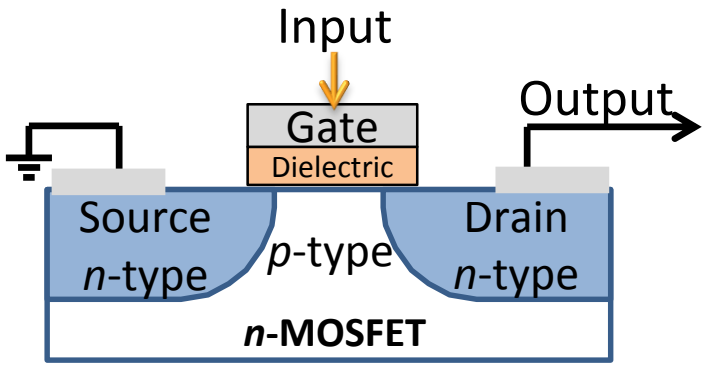
Transistor Transfer Characteristics

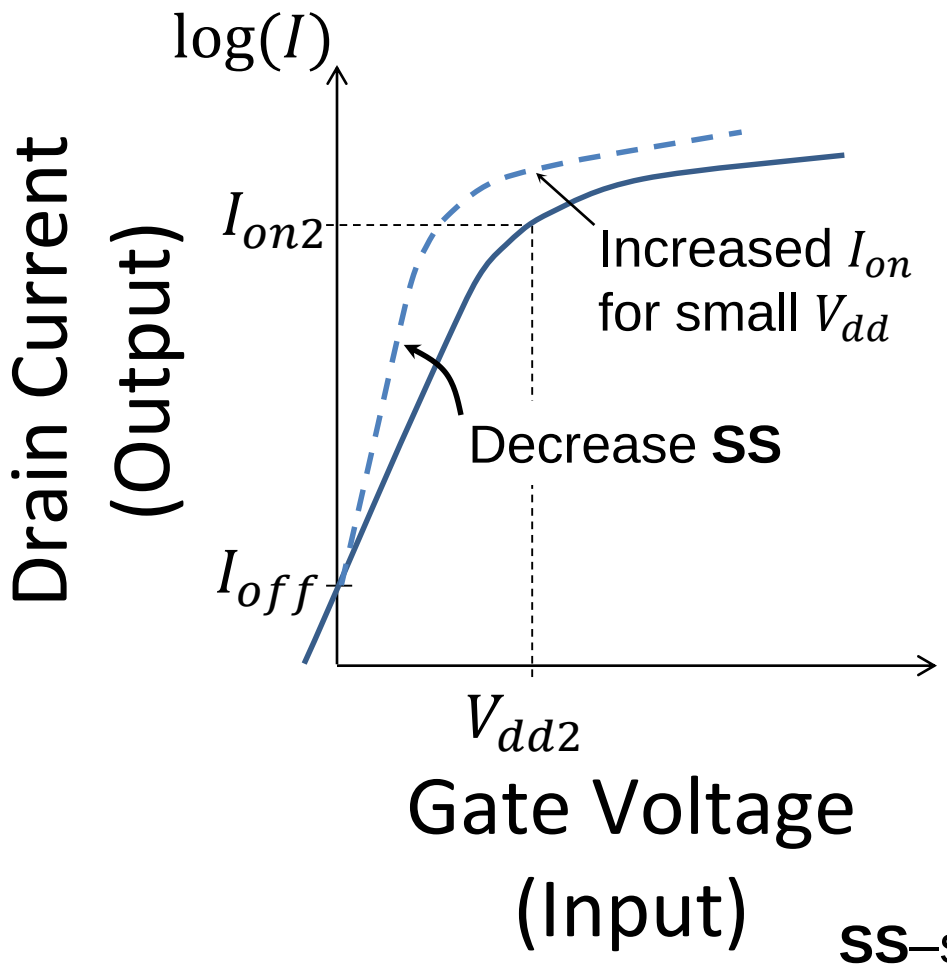


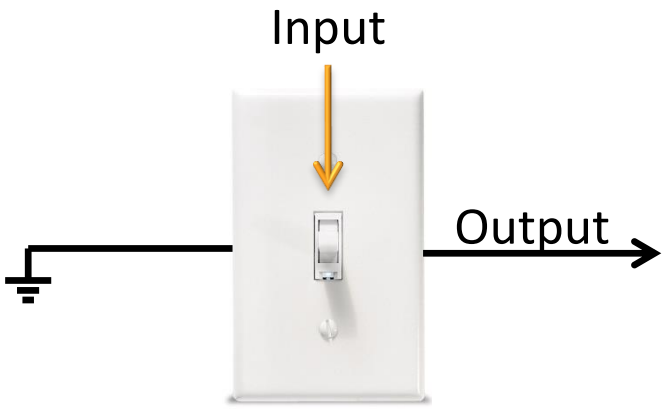


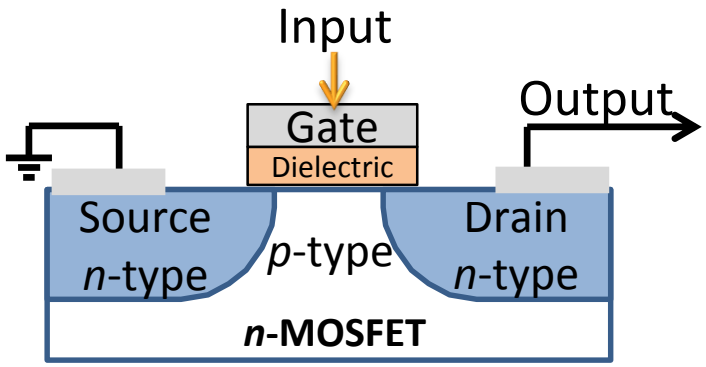


SS–subthreshold swing (mV/decade)

Transistor Transfer Characteristics



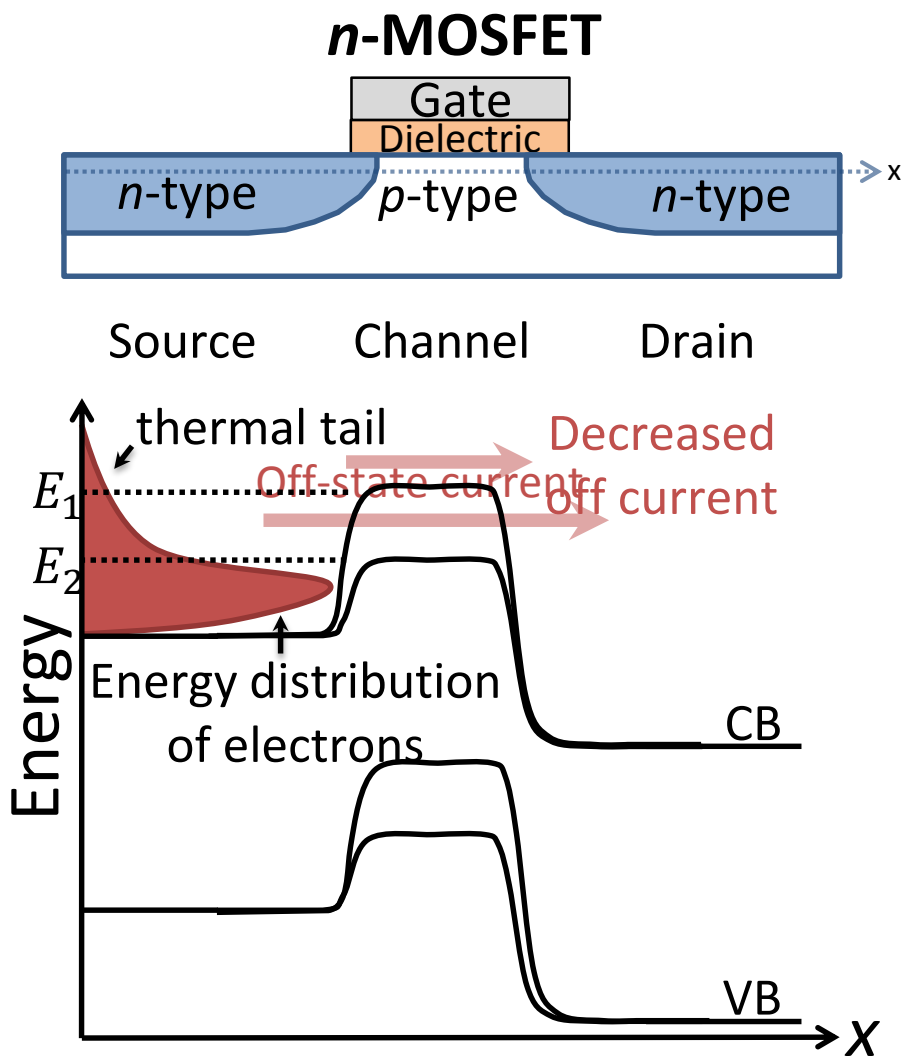




SS–subthreshold swing (mV/decade)

- If:
  - Reduce SS (subthreshold swing)
- Then:
  - $\downarrow V_{dd}$
  - $\downarrow P_{total}$

SS–Subthreshold Swing (MOSFET)



SS limited to
$60\ mV/decade$

Distribution of Electrons

$$n(E) = f(E) \cdot g_{DOS}(E)$$

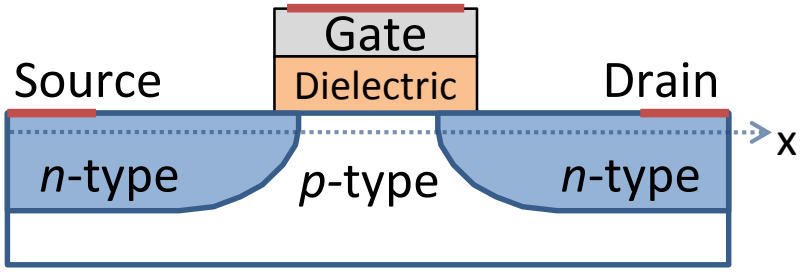
Fermi-Dirac Distribution

$$f(E) \approx \frac{1}{\exp\left(\frac{E - E_f}{kT}\right)}$$

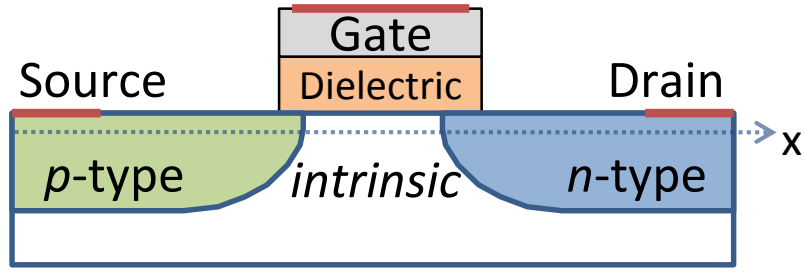
$$f(E) \Longrightarrow 60\ mV/decade$$

$$\frac{f(E_1)}{f(E_2)} \approx \exp\left(\frac{E_2 - E_1}{kT}\right)$$

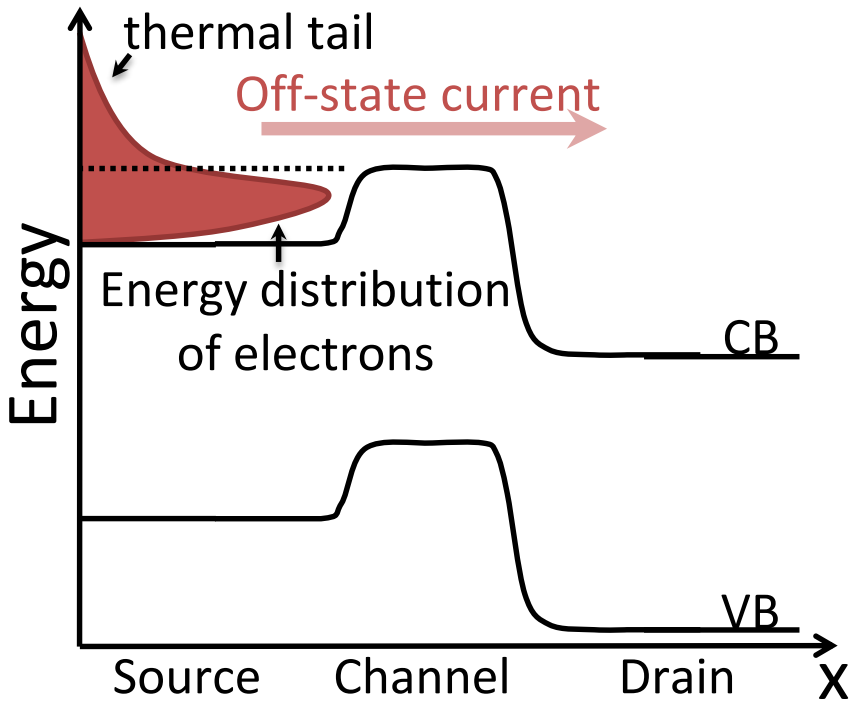
MOSFET and TFET Structures



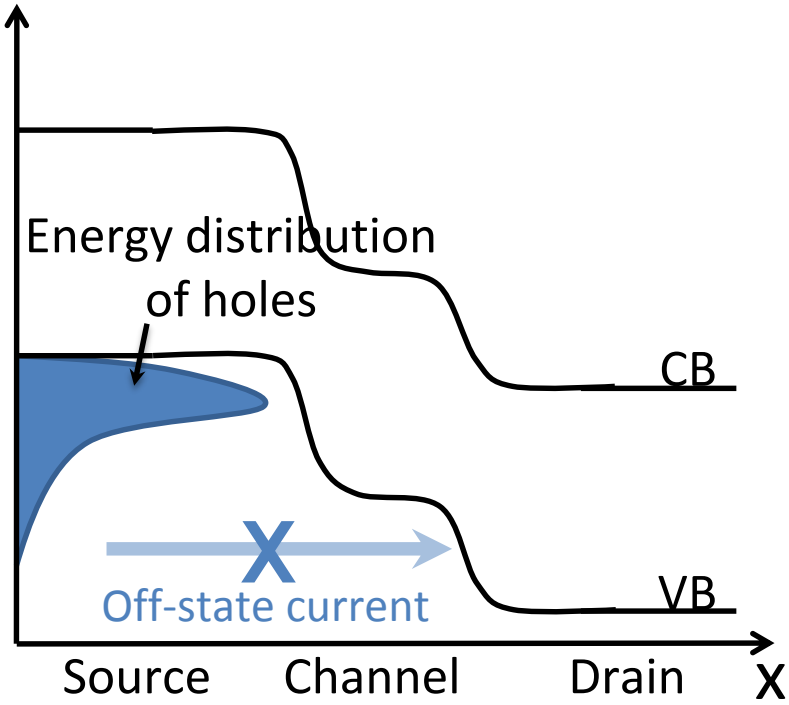
n-MOSFET



n-TFET

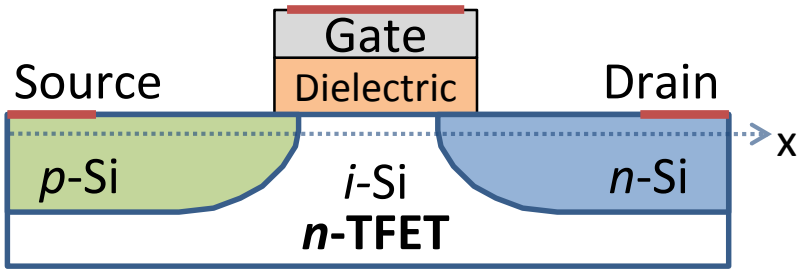


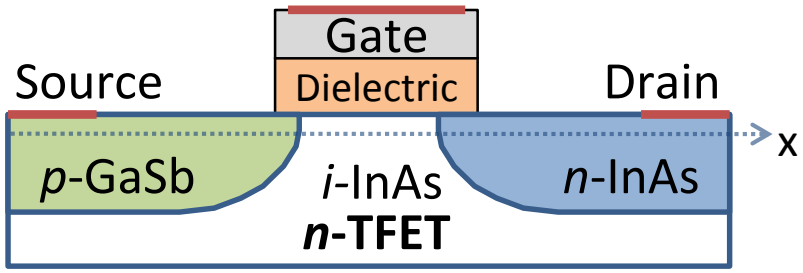
Limited SS of 60 $mV/decade$



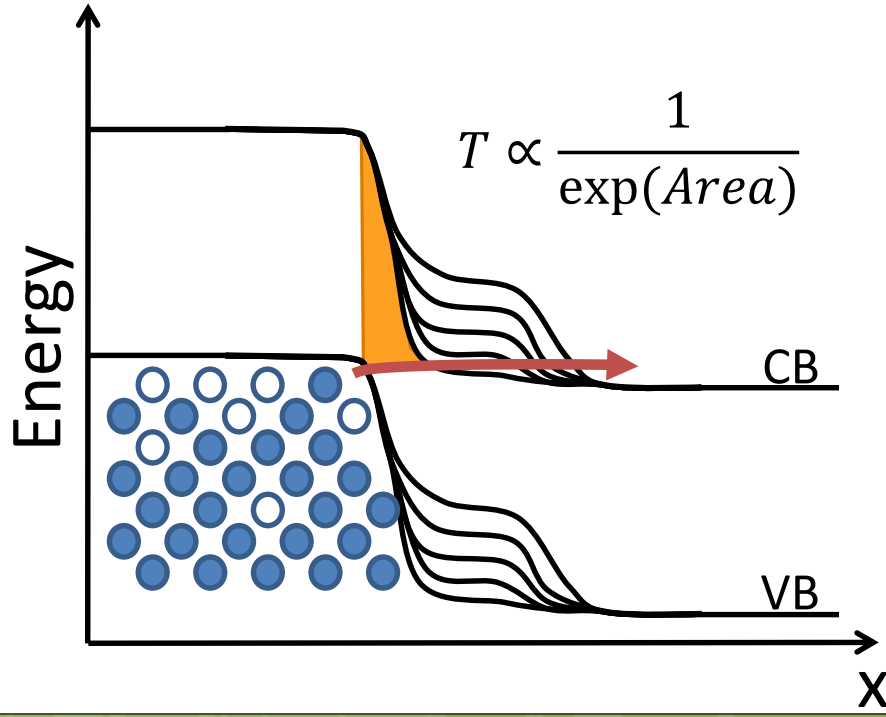
No 60 $mV/decade$ limit

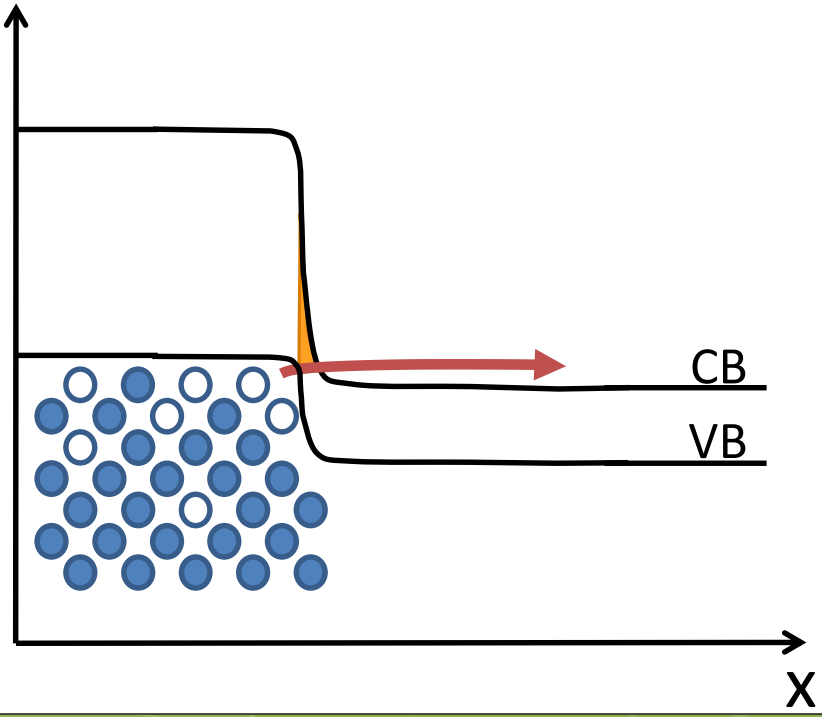
Tunneling in Homostructure Heterostructure





$$T \propto \frac{1}{\exp(Area)}$$





Experimental Results

Appenzeller: Carbon Nanotubes for High-Performance Electronics

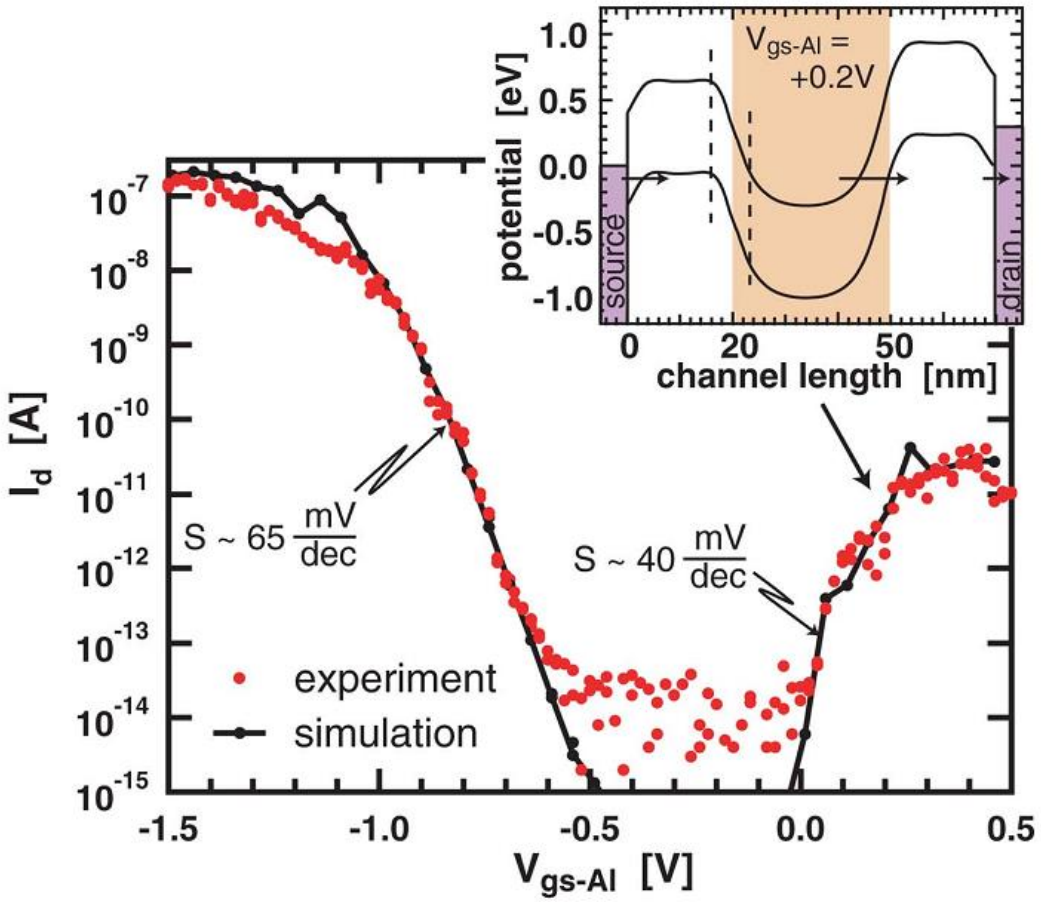
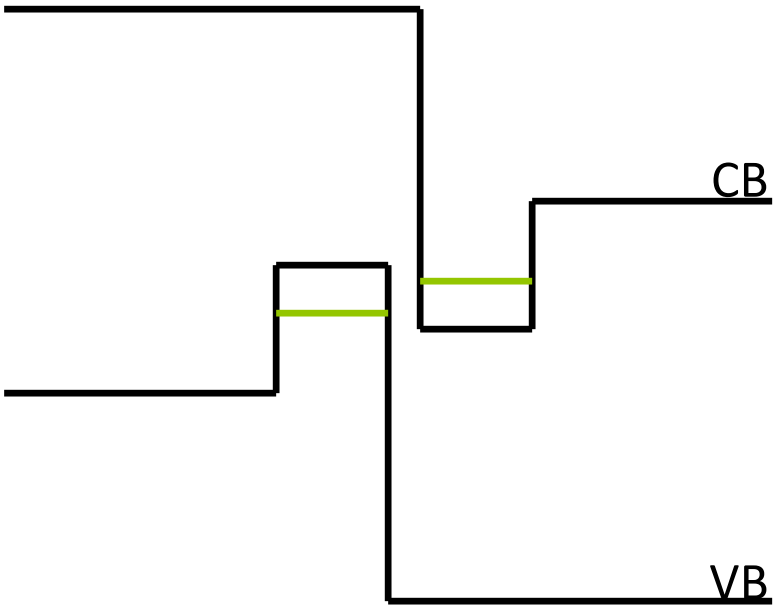


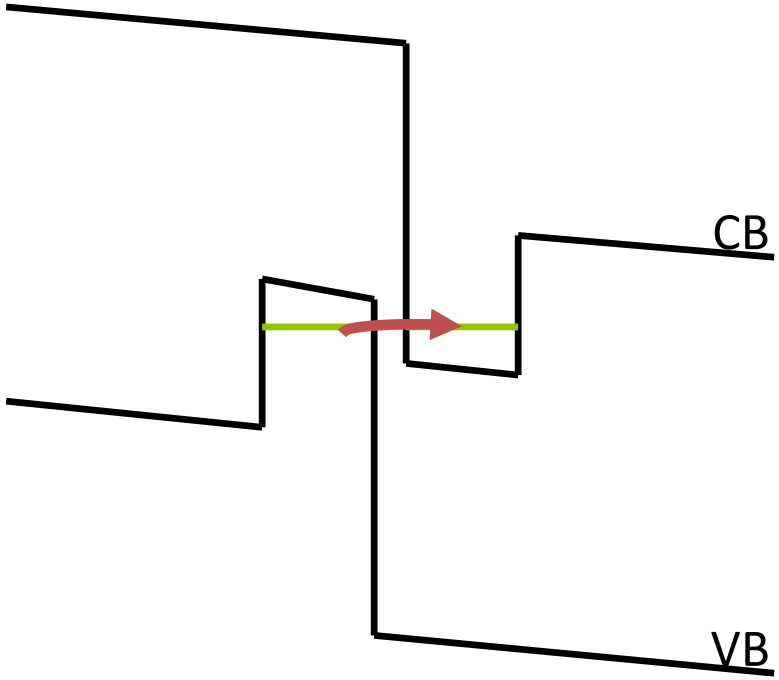
Fig. 12. *Experimental and simulated $I_{d(V_{gs-Al})}$ for a drain voltage of $V_{ds} = -0.5$ V and $V_{gs-Si} = -3$ V. The upper inset shows the band bending situation under tunneling conditions from the simulation.*

Density of States Switch

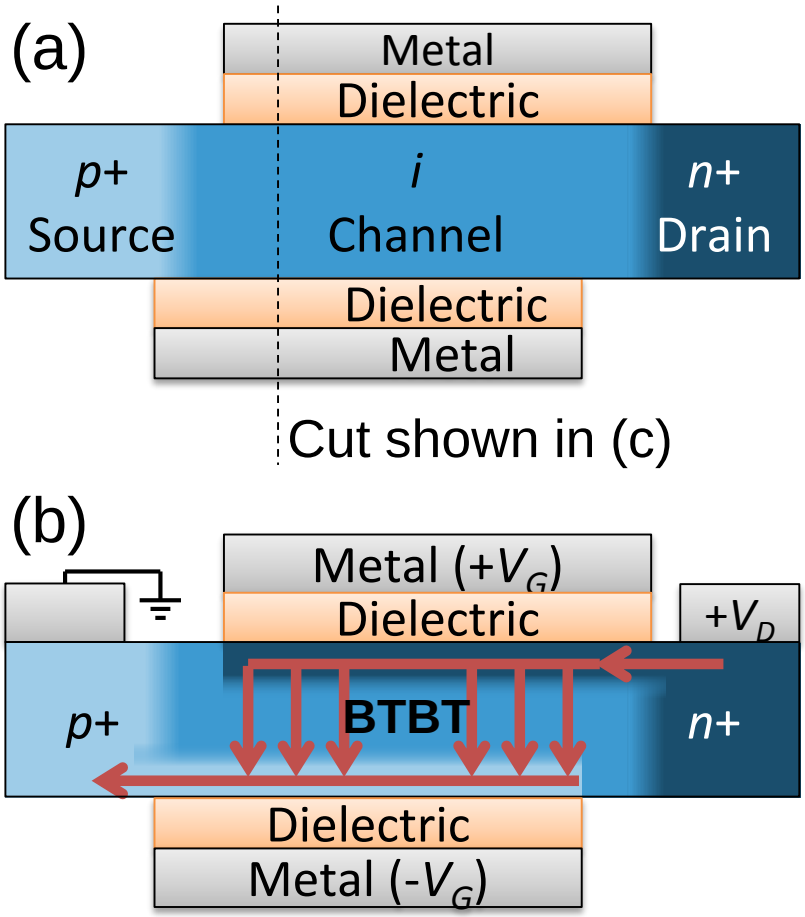
OFF-State

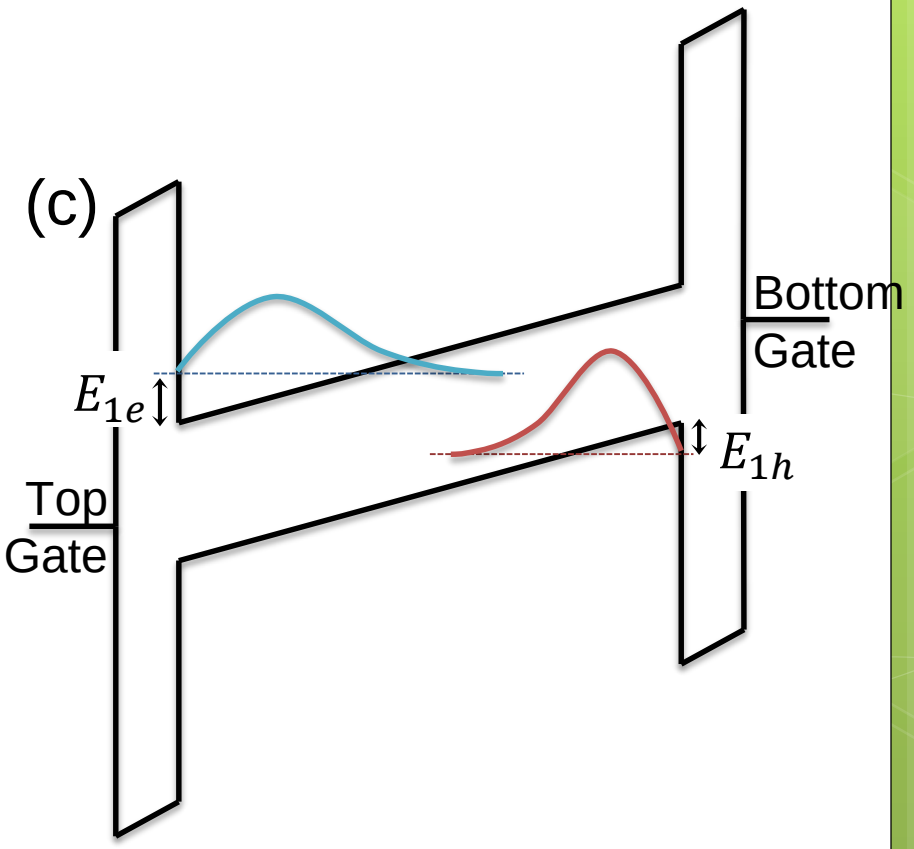


ON-State



Bilayer TFET Structure





Challenges Limiting TFET Performance

- Fundamental
  - Phonon effects
  - Band edge abruptness
- Technological
  - Interface states
  - Complex geometries, design
  - Junction abruptness
  - Thickness variation with thin body structures
  - Work function engineering

Summary

- Frequency and voltage scaling of MOSFETs have stalled due to power constraints
- Substantial voltage scaling requires new switching physics
- TFETs employ tunneling to overcome $60\ mV/decade$ limit
  - Experimental results have shown $\boldsymbol{SS} < 60\ mV/decade$, albeit at low currents
  - Much work is still needed in matching theory to experiment
- Heterojunctions and density-of-states switching designs may lead to better TFET performance
- We're currently exploring the bilayer TFET, which utilizes an interesting device geometry to create electron and hole quantum wells