Ultra-Thin, High Quality HfO$_2$ on Strained-Ge MOS Capacitors with Low Leakage Current

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Ultra-thin HfO$_2$ MOS capacitors on strained-Ge (s-Ge) have been fabricated with an extracted effective oxide thickness (EOT) of 4.9 Å and leakage current less than 0.2 A/cm^2 at $|V_G| < 0.5$ V. The CV measurements show little hysteresis and areal capacitance scaling for 50×50 to 200×200 µm^2 devices. A high series resistance is observed, likely due to a 500 meV valence band offset between the s-Ge and relaxed, p-type Si$_{0.55}$Ge$_{0.45}$ virtual substrate. The capacitance results suggest an extremely-scaled, high quality dielectric on s-Ge promising for deeply scaled CMOS.

Introduction

Strained-Ge (s-Ge) is a promising channel material for future CMOS nodes due to its very high hole mobility (1,2) and compatibility with existing processes. Compressive strain further increases the high hole mobility of Ge (2–5). In comparison to Si, high quality dielectric interfaces for Ge are challenging due to the lack of an ideal native oxide. Much work has been performed developing high quality dielectrics for Ge, and recently published results show scaled dielectrics for unstrained Ge (6,7) and s-Ge (7,8). In this work, for the first time, we show an extremely-scaled (EOT < 5 Å), high quality dielectric on s-Ge. CV measurements of a MOS capacitor structure show areal capacitance scaling, little hysteresis, and low gate leakage current (< 0.2 A/cm^2 for $|V_G| < 0.5$ V).

Fabrication

The epitaxial structure (shown in Fig. 1(a)) was grown by low-pressure CVD on a (100) p+ Si wafer. The epitaxial growth conditions were chosen to create a relaxed 1-µm Si$_{0.55}$Ge$_{0.45}$ virtual substrate (~10^{17} boron doped) on which a nominally 6-nm-thick s-Ge layer with no intentional doping was grown. The s-Ge layer is compressively strained (2.2% biaxial) due to the lattice mismatch with the relaxed Si$_{0.55}$Ge$_{0.45}$ virtual substrate. The s-Ge thickness is expected to be reduced to 3 nm after device processing.

The epitaxial wafer was cleaved into 3.2×3.2 cm pieces, and a 5-minute 1:10 (HCl:H$_2$O) clean was completed before atomic layer deposition (ALD). The ALD process consisted of 1 minute of O$_3$ followed by 38 cycles (~3 nm) of HfO$_2$ deposition (with TEMAH and H$_2$O as precursors), with both steps at 250 °C. This was followed by 400 cycles (~10 nm) of ALD TiN (with TiCl$_4$ precursor and N$_2$/H$_2$ plasma) at 300 °C. After ALD, 500 nm of Al was sputtered on the front side of the wafer. A five-minute (~5 µm) BCl$_3$/Cl$_2$ plasma etch was used to remove any epitaxial growth that may have occurred on the backside of the wafer, after which 1 µm of Al was sputtered on the backside of the piece. MOS capacitors were patterned using standard lithographic processes, and a final forming gas anneal (5% H$_2$, 95% N$_2$) was performed for 30 minutes at 450 °C. The final MOS capacitor structure (Fig. 1(a)) reflects the expected loss in the s-Ge due to the HCl clean and O$_3$ oxidation.
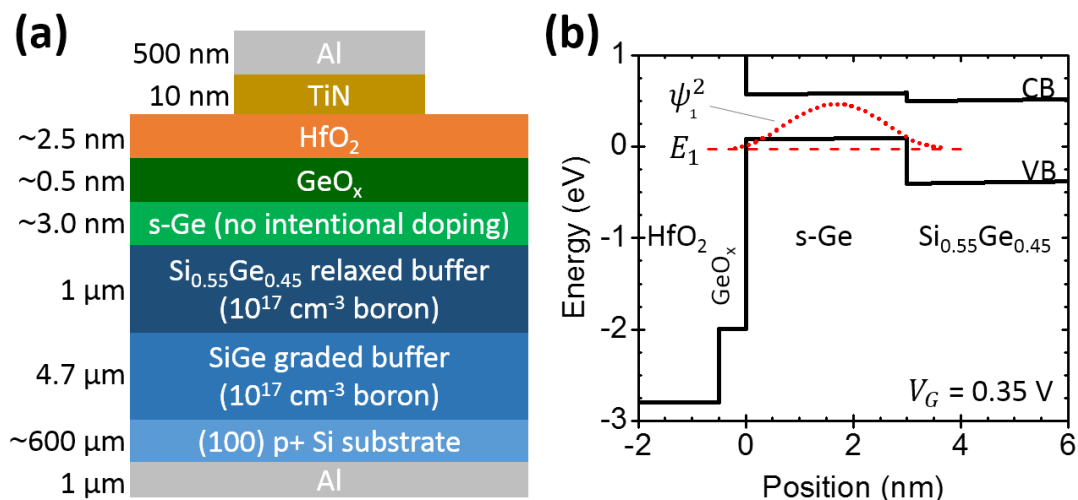
Figure 1. (a) Fabricated MOS capacitor structure with nominal thicknesses. (b) Energy band diagram of the simulated structure. Also shown are the first eigenenergy E_1 and first hole wavefunction density ψ_1^2 (shifted to align with E_1) as a function of position. ϵ_r=20 is used for both oxides in the simulation.

Electrical Results

CV measurements of a 100×100 µm MOS capacitor show an uncorrected, as-measured CET of 8.6 Å (7.7 Å after series resistance correction) at $V_{FB} - 0.7V$ (Fig. 2). Large frequency dispersion exists for frequencies > 50 kHz due to a high series resistance likely caused by a 500 meV valence band offset (9) between s-Ge and $Si_{0.55}Ge_{0.45}$ (Fig. 1(b)). The IV measurements (Fig. 3) show low gate leakage current ($|J_G| = 0.17$ A/cm^2 at $V_G = -0.5$ V), which translates to $I_G = 17$ pA/µm for $L_G = 10$ nm, well below the ITRS off-state requirements of ~100 A/cm^2 for high performance and low operating power devices (10).
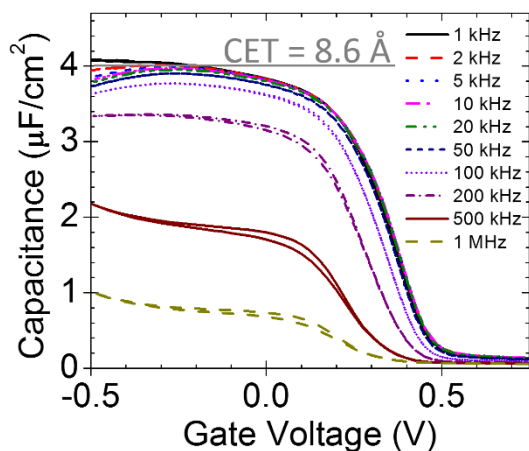

Figure 2. Measured CV curves for a 100×100 µm^2 s-Ge MOS capacitor fabricated with 1 minute of O_3 and 38 cycles of HfO$_2$. The plot shows little hysteresis and an 8.6-Å as-measured CET at $V_G = -0.5$ V.
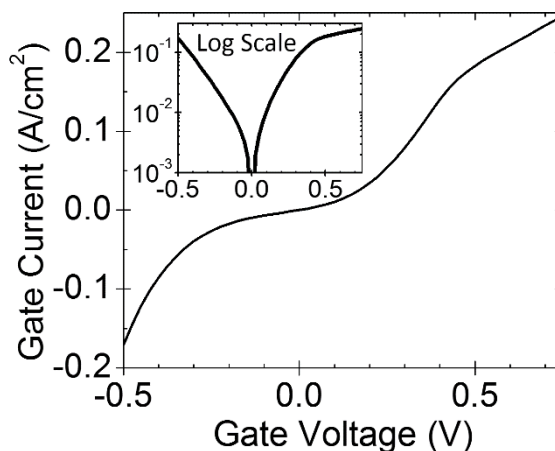
Figure 3. Measured gate leakage for the s-Ge MOS capacitor shown in Fig. 2. The inset shows gate current on a log scale. Small gate leakage ($|J_G| < 0.2$ A/cm^2) is observed for $|V_G| < 0.5$ V.

Two additional MOS capacitor samples were fabricated, and details are shown in Table 1. The gate leakage current for all three devices is shown in Fig. 4. A ~20× reduction in leakage current is seen by increasing the number of HfO_2 ALD cycles from 38 to 44 and from 44 to 50.

Material	Pre-ALD clean	ALD process	CET (Å)	EOT (Å)
s-Ge on $Si_{0.55}Ge_{0.45}$	1:10 $HCl:H_2O$	1 min O_3 **38 cycles** HfO_2 400 cycles TiN	8.6	4.9
	None	1 min. O_3 **44 cycles** HfO_2 400 cycles TiN	9.3	5.7
	None	1 min. O_3 **50 cycles** HfO_2 400 cycles TiN	10.3	6.8

Table 1. Details for the three fabricated s-Ge/GeOx/HfO_2 MOS capacitor wafers.
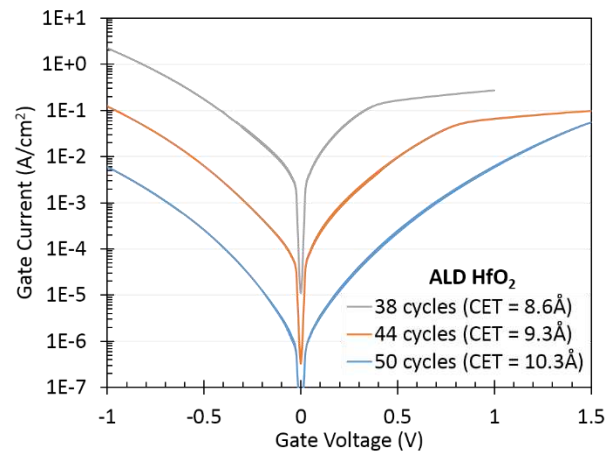
Figure 4. Measured gate current for different HfO_2 thicknesses.

Simulation and Modeling

Quasistatic one-dimensional self-consistent coupled Poisson-Schrödinger electrostatic simulations were performed in order to extract EOT of the experimental devices. A strain-dependent 6×6 $k \cdot p$ Hamiltonian (with deformation potentials from (9)) was used to calculate hole quantization in the s-Ge layer. In accordance with (11), a 2.1 eV valence band offset between Ge and GeO_x was used in the simulations (Fig. 1(b)). The 500 meV valence band offset between s-Ge and $Si_{0.55}Ge_{0.45}$ creates a deep quantum well confining most of the holes in the s-Ge layer (9).

The simulated CV curves were quite insensitive to s-Ge thickness and SiGe doping level. Decreasing the s-Ge thickness from 5 to 3 nm resulted in a marginally steeper rise in the simulated capacitance when transitioning from hole depletion to accumulation, but the extracted EOT was not significantly affected. The simulations shown in this paper use 3-nm s-Ge thickness and 10^{17} p-type doping in the SiGe layer, consistent with experimentally expected values.

Fig. 5 shows the 10 kHz experimental CV (for 38 cycles of HfO_2) with simulated quasistatic CV curves for structures with varying EOT. The mismatch of the simulated and experimental curves in strong hole accumulation is due to both a large series resistance ($R_s \sim 0.1\ \Omega\cdot cm^2$) and large gate conductance ($G_t \sim 0.4\ S/cm^2$ at $V_G = -0.5$ V), which causes a sizable error when transforming the measured impedance to a two-element parallel capacitance C_P, parallel conductance G_P circuit model (12).

A circuit model incorporating parasitic gate tunneling conductance G_t and series resistance R_s (inset of Fig. 6) is applied to an ideal simulated CV in order to recover the measured CV result yielding an extracted EOT of 4.9 Å (Fig. 6). This is the smallest known EOT for a high quality dielectric on s-Ge published to date. Other recent results include 7-Å, 9-Å, and 10-Å EOT on s-Ge (7,8,13), and an 8-Å CET on unstrained Ge (6).
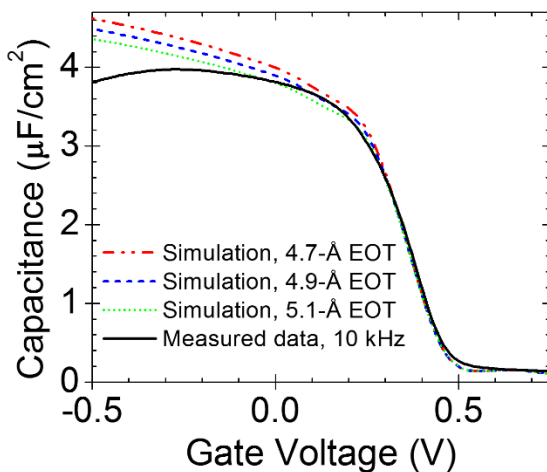
Figure 5. Simulated quasistatic CVs for the structure shown in Fig. 1(b) with varying EOT and measured CV for a MOS capacitor with 38 cycles of HfO_2 (multi-frequency CV shown in Fig. 2). A large series resistance in addition to gate leakage causes deviation between measurement and simulation in strong hole accumulation.
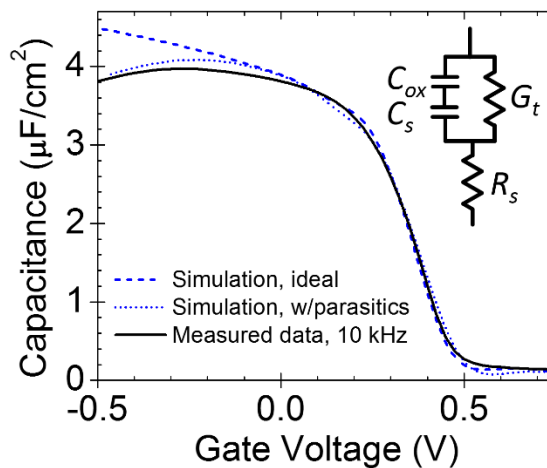
Figure 6. Simulated CV for a 4.9-Å EOT. The inset shows the circuit model used to correct for parasitics. Parasitic tunneling conductance G_t and series resistance R_s are applied to the ideal simulation to recover the measured CV. R_s and G_t were extracted by comparing DC and HF (200 kHz) measured conductance.

Benchmarking

Fig. 7 compares the gate current as a function of EOT for MOS capacitors fabricated in this work and by Zhang (7,14). Thinner EOT is achieved by replacing Al_2O_3 with HfO_2, due to HfO_2's larger relative permittivity. The figure shows an exponential increase in gate current with decreasing EOT. Gate leakage current obtained in this work is comparable with previous results on bulk and s-Ge.
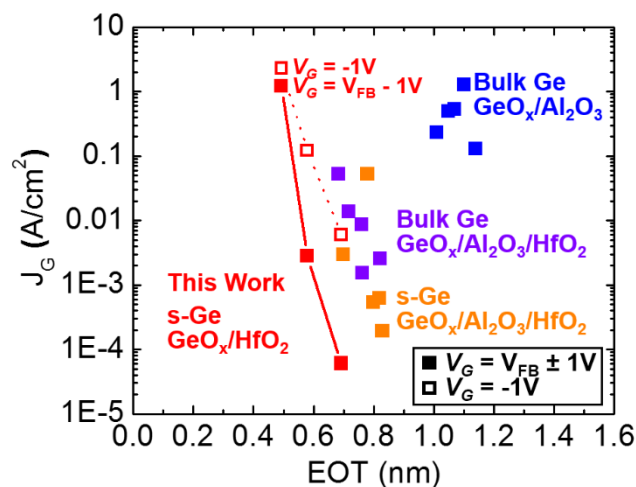

Figure 7. Gate current as a function of EOT for capacitors in this work (red symbols) and Zhang's (7,14). In keeping with previous publications, the gate current is given at V_{FB} + 1V for n-type and V_{FB} − 1V for p-type material (both shown with closed symbols) in order to compare devices at similar carrier densities. However, the comparison is imperfect because

V_{FB} varies due to different 1) work function metals, 2) substrate doping, and 3) dielectric charges, such that the absolute gate voltage can vary significantly for different data points. The devices in this work are also compared at a fixed $V_G = -1V$ (open symbols) to account for V_{FB} differences, which brings this work's results in line with previous data.

Summary

In summary, s-Ge/GeO$_x$/HfO$_2$ MOS capacitors (with O$_3$ surface passivation) demonstrated a 4.9-Å EOT and low gate leakage < 0.2 A/cm^2 at $|V_G| < 0.5$ V. The capacitors show little hysteresis, but significant frequency dispersion due to a high resistance caused by a large 500 meV valence band offset between s-Ge and the Si$_{0.55}$Ge$_{0.45}$ substrate. An exponential decrease in gate leakage current is shown for increasing HfO$_2$ ALD cycles. The results show a promising ultra-scaled, high quality dielectric on s-Ge with low leakage current.

Acknowledgments

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