Electrostatic Design of Vertical Tunneling Field-Effect Transistors

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Tunneling field-effect transistors (TFETs) have created excitement for their potential to overcome the 60 mV/decade thermal limit of the subthreshold swing for conventional devices enabling lower power electronics. However, as shown in the TFET review by Seabaugh and Zhang [1], experimental subthreshold characteristics have not achieved the steepness of theoretical predictions. Possible explanations for the non-abrupt turn-on of experimental devices include long band-tails (exacerbated by doping) that extend into the semiconductor band gap, mid-gap and interface trap-states, inhomogeneity of the semiconductor composition, strain and/or thickness, and non-optimal electrostatic design of the transistor structure. This paper focuses on improving the electrostatic design of vertical tunneling structures (where tunneling occurs vertically toward the gate), in order to better experimental turn-on characteristics.

Un-optimized electrostatic design of TFET structures can contribute to significant slope degradation seen in experimental devices. The slope degradation is often not captured in device simulations due to poor calibration of the band-to-band tunneling (BTBT) tunneling parameters, which exponentially affect the tunneling rates*. Furthermore, theoretical analysis of tunneling (such as the authors' works [2], [3]) often neglects two-dimensional effects such as the parasitic tunneling path at the focus of this paper.

Figure 1 shows two related vertical TFET designs: the air-bridge and pillar structures. Advantages of these vertical structures include 1) tunneling aligned with the gate electric field for enhanced gate modulation, 2) a two-dimensional tunneling area for increased current-drive, and 3) elimination of direct source-to-drain leakage paths, which excludes designs in which the *p* layer extends all the way to the drain. Vertical TFETs have been fabricated using the direct-gap *p*+InP/*n*+InGaAs, *p*+AlGaSb/*n*-InAs, and *p*+GaSb/*n*-InAs material systems [4]–[6], but the results of this paper are general and can be applied to most vertical *p*-*n* homo- or heterostructures. The ON-state of such structures is achieved when sufficient gate bias is applied such that the conduction band (CB) of the *n* layer lies below the valence band (VB) of the *p* layer so that electrons tunnel from the *p* layer VB to the *n* layer CB.

Non-vertical tunneling paths exist in the OFF-state (Figure 1), which degrade the switching characteristics. The *p*+ layer depletes the thin *n*- material directly above it; however, where the *p*+ layer is absent, the *n*- material is not depleted, which results in a lower CB energy. Electrons from the *p*+ VB initially tunnel diagonally at the device edges to the lower CB before tunneling vertically at larger gate bias (Figure 2). The diagonal parasitic tunneling paths have a longer tunneling distance and lower electric field compared to pure vertical tunneling which result in smaller currents (Figure 3). Once sufficient gate bias is applied, vertical tunneling dominates due to the larger tunneling area, smaller tunneling distance, and larger electric field.

Figure 3 depicts the impact of the parasitic tunneling paths on the overall transfer characteristics. While the turn-on of each leakage path is individually sharp, the sum of all the paths results in a degraded transfer characteristic. In order to realize abrupt switching, the parasitic paths—caused by the large *horizontal* electric field created by the abrupt termination of the *p*+ layer—must be eliminated. Direct source-to-drain leakage will result if the *p*+ layer extends to the drain. If one could control the lateral doping profile, such that the *p*+ layer gradually became intrinsic towards the drain-end, these parasitic paths could be avoided, but processing and material limitations restrict this in practice.

The bilayer device, depicted in Figure 4a, could be used to overcome the challenges of parasitic tunneling paths enabling study of the fundamental switching abruptness of tunneling devices. The device is *electrostatically* doped through the use of top and bottom gates. The *electrostatic* doping prevents long band-tails introduced by heavy acceptor and donor doping, and also allows lateral control of the hole-rich layer at the bottom of the device through the design of the bottom gate. Increasing the thickness of the bottom oxide reduces the lateral field at the right edge of the bottom gate, which helps prevent diagonal tunneling. The energy band diagram of the structure (Figure 4b) shows that lateral tunneling can be greatly reduced.

In summary, un-optimized electrostatic design of vertical TFETs can lead to parasitic tunneling paths that can seriously degrade the slope of the transfer characteristics. The bilayer device design is suggested to minimize parasitic diagonal tunneling so that the fundamental switching abruptness of vertical TFETs can be effectively studied.

*The BTBT rate is often modeled as $R_{net} = AF^P exp(-B/F)$, where R_{net} is the net recombination rate, F is the electric field, and A, B, and P are model parameters. As B is increased, tunneling at low fields decreases sharply due to the exponential dependence, and the majority of tunneling occurs only at high fields. Simulations may show that only purely vertical BTBT (and not parasitic diagonal tunneling) occurs in a device structure with specific tunneling parameters, but this may not represent the actual tunneling physics in a physical device.

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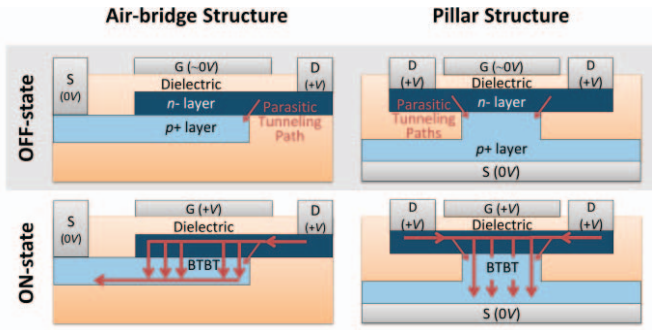

Figure 1. Diagram of the air-bridge and pillar structures in the OFF- and ON-states. The red arrows indicate BTBT currents. Both structures suffer from diagonal parasitic tunneling that limits OFF-state current and degrades the switching abruptness.

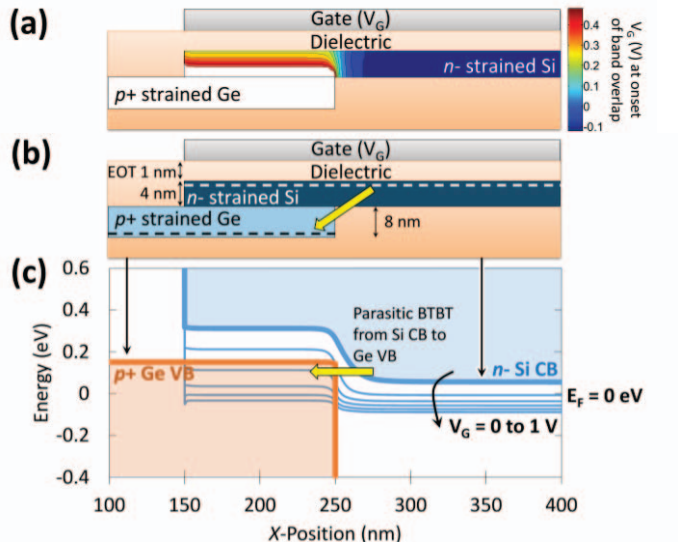

Figure 2. The horizontal axes of (a)-(c) are aligned and all plots assume zero source and drain bias. (a) Gate voltage (V_G) at which the *n*- strained-Si CB first overlaps in energy with the *p*+ strained-Ge VB as a function of position in the device. Overlap of the CB directly above the *p* layer requires an additional 0.3V of V_G compared to the undepleted *n* region to right of the *p* layer. The simulation was computed neglecting quantization. (b) Diagram of the air-bridge structure in the OFF-state for the strained *p*+Ge/*n*-Si material system. Vertical dimensions of the simulated structure are provided. (c) Simulated energy band diagram as a function of horizontal position in the device [7]. The VB is plotted for the bottom of the 5e19 cm^{-3} *p*+ Ge layer while the CB is plotted for the top of the 1e18 cm^{-3} *n*- Si layer as indicated by dashed lines shown in (b). Increasing gate voltage (V_G) lowers the Si CB energy, but does not affect the VB at the bottom of the Ge layer due to its heavy doping and distance from the gate. The rise in the CB energy for $x < 250$ nm is caused by depletion of the *n*- Si due to the *p*+ layer. The yellow arrows indicate the diagonal parasitic tunneling path that limits the OFF-state current and switching abruptness.

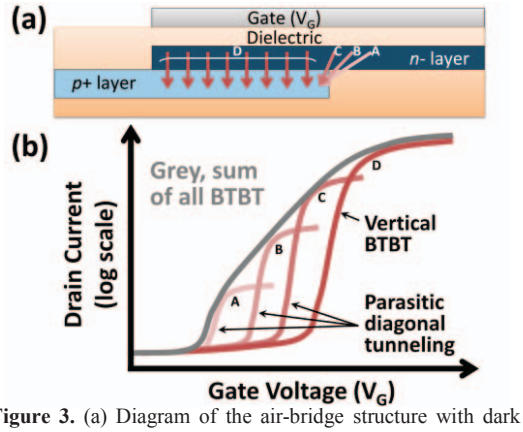

Figure 3. (a) Diagram of the air-bridge structure with dark red arrows (labeled D) indicating the desired vertical BTBT path and light red arrows (labeled A-C) indicating parasitic tunneling paths. (b) Sketch of drain current versus gate voltage for a hypothesized device. The colored curves represent the contribution of each of the tunneling paths depicted in (a). Each individual tunneling path generates a steep slope, but the summation of all the tunneling paths (grey curve) results in a very gradual turn-on. Parasitic tunneling paths must be eliminated in order to realize a steep turn-on.

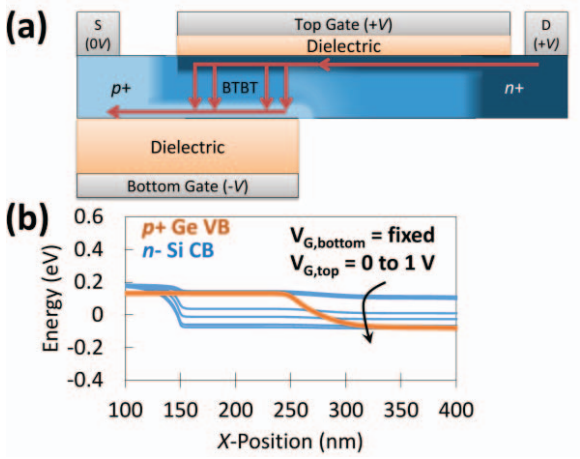

Figure 4. (a) Bilayer TFET structure. The top and bottom gate are biased oppositely in order to create an electron-rich layer near the top gate and a hole-rich layer near the bottom gate. BTBT occurs when a sufficiently large bias is applied between the top and bottom gates such that CB near the top and VB near the bottom overlap in energy. The red arrows indicate the current path. A thicker dielectric is used for the bottom gate to minimize the lateral field at the right side of the bottom gate to minimize parasitic diagonal tunneling. (b) Energy band diagram of the structure shown in (a). The parasitic diagonal tunneling path has been greatly mitigated through optimal electrostatic design of the bilayer structure.