Effect of Uniaxial Strain on the Drain Current of a Heterojunction Tunneling Field-Effect Transistor

Paul M. Solomon, I. Lauer, A. Majumdar, J. T. Teherani, M. Luisier, J. Cai, and S. J. Koester

***Abstract*—The electrical characteristics of a heterojunction tunneling field-effect transistor (HETT), with a p-type Si$_{0.75}$Ge$_{0.25}$ source, have been measured as a function of strain. HETTs with channel transport and applied strain both in the [110] direction show a smooth monotonic change in drain current over a range of 0.09% compressive to 0.13% tensile strain. A measure $\gamma = (d/d\ln J_D)(d\ln J_D/ds)|_{s=0}$ of the effect of strain s on tunneling current J_D is proposed, which captures the dependence of the tunneling exponential argument on strain. An experimental value of $\gamma = -11.7$ is extracted for the tensile case and compared to simulation results. We found theoretically that the value and sign of γ depend sensitively on the built-in strain at the Si–SiGe interface.**

***Index Terms*—Band-to-band tunneling, strain, stress, tunneling FET (TFET).**

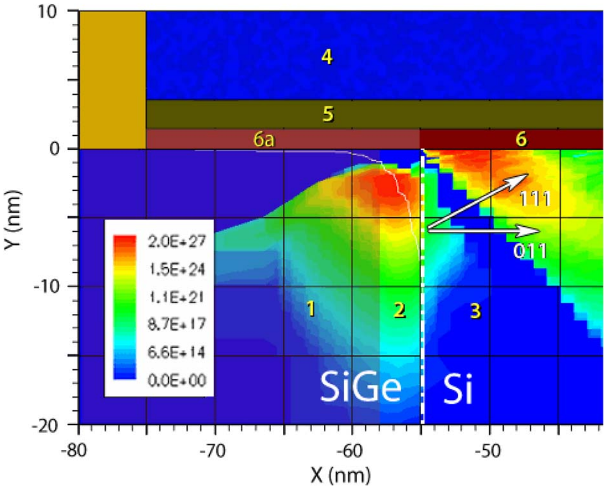

Fig. 1. Schematic cross section near the tunneling source region of HETT device, with carrier generation regions superimposed. (1) p+ (shaded) doped and (2) undoped Si$_{0.75}$Ge$_{0.25}$ sources, (3) undoped Si channel, (4) polysilicon gate, (5) HfO$_2$ and (6) SiO$_2$ gate insulator layers, and (6a) SiO$_2$ layer in gate-overhung region, in place for SiGe growth. The band-to-band generation rate (in cm^{-3}/s) is superimposed on the device cross section. The arrows show the crystal direction.

I. Introduction

The TUNNELING field-effect transistor (TFET) or heterojunction tunneling field-effect transistor (HETT) has been intensively investigated as a possible replacement for conventional CMOS transistors in low-power applications because of predictions [1] that the nonthermal band-to-band-tunneling injection mechanism will lead to a steeper subthreshold slopes. It would be desirable to fabricate TFETs using group-IV-based materials due to their compatibility with standard CMOS technology. The SiGe source/Si channel heterojunction enhances tunneling both due to the lower bandgap of the SiGe source and because of the staggered band alignment between SiGe and Si [2]. To date, there have been very few studies of the effect of externally applied strain on the performance of TFETs. Applied strain has the potential to improve the drive current in TFETs, and careful studies of the strain effect could also lead to improved understanding of the band-to-band-tunneling mechanism. Guo *et al.* [3] reported all-silicon TFETs with strain applied along the [110] direction (the transport direction was also [110]) using a bending apparatus. The authors observed a nonmonotonic dip in the drain current response at zero strain, which was attributed to the density of states spike simulated in [4] and could also be due to band crossings due to strain of plane conduction-band minima [5]. In this letter, we study the effect of uniaxial strain on the drain current of the Si/SiGe HETT and elucidate the tunneling mechanism (which is very complex in these materials due to the many bands participating). Our observations differ from those in [3], and we propose a new parameter γ that quantifies the effect of strain on tunneling current and is utilized to provide physical interpretation for the observed behavior.

II. Device Fabrication and Electrical Measurements

The schematic cross section near the source of the HETT considered in this letter is shown in Fig. 1. The fabrication sequence closely follows a standard CMOS flow with a high-k gate dielectric except that the source and drain regions of the device are masked separately, allowing n-type implantation of the drain region and an *in situ* doped p-type Si$_{0.75}$Ge$_{0.25}$ epitaxial source layer to be grown in a recess which undercuts

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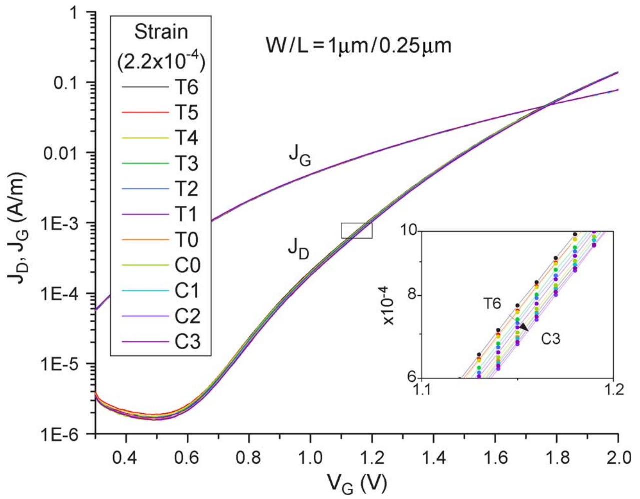

Fig. 2. Drain and gate characteristics of a 1×0.25 μm^2 HETT under the specified stress conditions of bending strain. The strain T6-C3 is in units of 2.2×10^{-4} (1/12 turn) tensile–compressive.

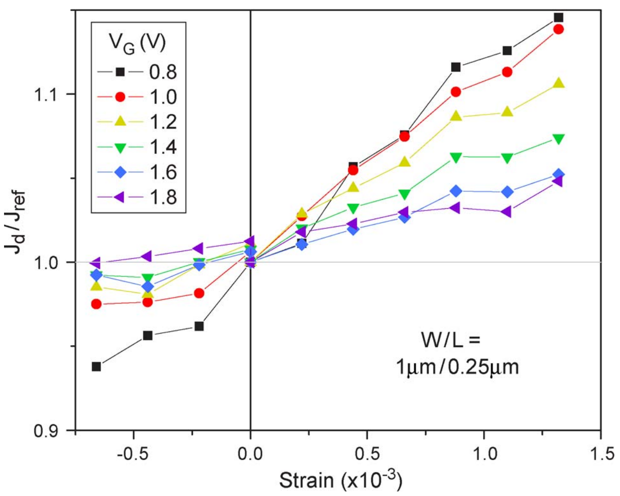

Fig. 3. Normalized drain current versus applied strain for the 1×0.25 μm^2 HETT. Strain is along the [110] (channel) direction and is positive for tensile and negative for compressive strains, respectively. Drain current is normalized to unity at zero strain (tensile) and smoothed using a 16-point binomial smoothing.

the gate. This places a lateral tunnel junction directly under the gate. As in [3], devices were aligned along the [110] direction on a (100) silicon surface. While a range of devices were measured, the results reported utilized two devices having W/L values of 2/0.3 and 1/0.25 (μm/μm), respectively. The band-to-band generation rates shown in Fig. 1 were simulated using Synopsis S-Device [6] with parameters adjusted to match the experimental I_d-versus-V_g characteristic. These simulation results are used here to gauge the direction and location of the tunneling path with respect to the SiGe/Si interface.

Electrical measurements were made using an HP 4145B parameter analyzer under bending stress applied along the channel direction using a bending apparatus designed by Scott Thompson, University of Florida, that was calibrated with a strain gauge. Since the configuration of this apparatus is changed between compressive and tensile stress measurements, extra care was taken to perform measurements near the zero-stress condition in both cases. Drain and gate current characteristics are shown in Fig. 2. For these devices, the gate current I_g was larger than the drain current I_d. The large I_g was due to the leakage across the oxide in the recess region (6a in Fig. 1) which, as confirmed by transmission-electron microscopy, was thinned during the gate recess process. While undesirable, this leakage does not affect I_d.

The sensitivity of the drain current to the applied strain is shown in Fig. 3. In spite of stringent efforts, some drift in the measurements is evidenced by the differences between the data points at zero strain compressive versus zero strain tensile.

III. DISCUSSION

The dependence of the drain current on strain is quite smooth and regular, apart from obvious drift and noise, and unlike in [3], no anomalies are seen about the zero strain point. We suspect that the zero strain point in [3] is subject to the same difficulties that we experienced and is likely an artifact. It is true that our FET has a SiGe rather than Si source compared to that [3], and our gate lengths were shorter, but these differences are unlikely to account for the qualitatively different results implied by that single zero-strain point. Indeed, apart from this point, our results are quite similar to those in [3].

As can be seen in Fig. 3, the sensitivity to strain is greater at lower gate voltages. This is due to the dependence of the tunneling current on the argument of an exponential (the WKB action integral), which is larger at lower currents due to lower fields, hence larger tunneling distances, that contains strain-dependent parameters such as effective mass and bandgap. Expressing the tunneling current as

$$J_D = J_\infty e^{-H(s)} \tag{1}$$

where we assume that J_∞ is a constant, s is the strain, and $H(s)$ is a strain-dependent argument that is equal to double the action integral in tunneling parlance. In standard tunneling theory [7], $H \propto m_r^{1/2} E_g^{3/2}$, where m_r is the reduced effective mass and E_g is the bandgap. Tunneling in materials such as silicon is more complicated, involving the full complex band structure [8]. In an attempt to capture this generality, we assume an action integral in the form of a product of various band-related parameters p raised to a power α, i.e., $H = b \prod_i p_i^{\alpha_i}$, where b is a constant. We derive

$$\frac{d \ln J_D}{ds} = -H(0) \sum_i \frac{\alpha_i}{p_i} \frac{dp_i}{ds} = -\gamma H_0 \tag{2}$$

where $H_0 = H(0)$ and γ is the total sensitivity to strain of the exponential argument expressed as a sum of the individual parameter sensitivities. Eliminating H_0 from (2) using (1), we get

$$\frac{d \ln J_D}{ds} = \gamma(\ln J_{D0} - \ln J_\infty). \tag{3}$$

Therefore, by plotting $d(\ln J_D)/ds$ versus $\ln J_{D0}$, one should get a straight line intersecting the ordinate at $\ln J_\infty$ and with a slope of γ. This approach assumes that a single set of bands

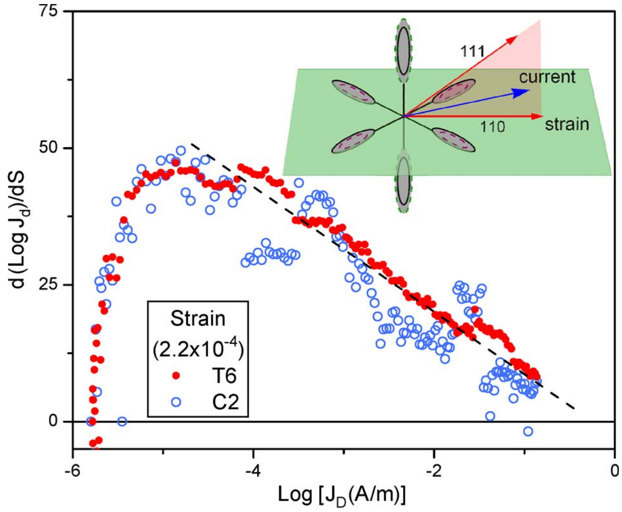

Fig. 4. Sensitivity of J_D to strain is plotted against $\log J_D$ for tensile and compressive cases (T6 and C2) for the 1×0.25 μm^2 HETT. The sensitivity parameter γ is the slope, as indicated by the dashed line. The inset shows a schematic diagram of the conduction-band lobes in the silicon with the effect of strain indicated by the dashed lines, showing an energy lowering (expansion) for the out-of-plane and an increase (contraction) for the in-plane lobes. The drawn plane indicates the wafer surface.

dominates the tunneling process over the range of interest, and that currents are low enough that the tunneling current strain dependence is dominated by the exponential term and not the prefactor.

Strain tensor analysis and imaginary band calculations were performed for the system, as shown in Fig. 1, and values of γ were derived from the action integrals assuming, for simplicity, a uniform field. The imaginary band calculations were made using a nearest neighbor sp^{3}d^{5}s* tight-binding model with spin-orbit coupling [9] that incorporates any arbitrary strain tensor into the band-structure calculation. Strain was incorporated by displacing the atoms from their equilibrium positions according to any arbitrary stress tensors. The strain parameters are taken from [10]. It was found that the value of gamma was very sensitive not only to the tunnel direction but also to the built-in (mismatch) strain in the SiGe. For instance, assuming a biaxial strain in the plane of the wafer gives the opposite movement of the valence band edge of the SiGe with uniaxial strain compared to biaxial strain in plane of the SiGe recess sidewall. Thus, our experimental results are consistent with the biaxial strain in the plane of the sidewall, with the vertical face of the recess being the template for the growth of the epitaxial SiGe. Similarly, the Si conduction-band contributions to the action integral are very sensitive to the tunnel direction reversing for the 111 compared to 011 directions. This is because (see Fig. 4 inset), in the 011 transport direction, the two out-of-plane conduction-band lobes, which have a negative strain sensitivity, dominate the tunneling, whereas in the 111 direction, the four in-plane lobes, having a positive sensitivity, give the major contribution. The best (most negative) theoretical γ was -7.0 for a direction $\sim 20^\circ$ above the 011 plane, which agrees very well with the tunneling direction in Fig. 1 simulations. While this is still less than the experimental value (-11.7), we consider this to be very satisfactory given the experimental and theoretical uncertainties.

IV. CONCLUSION

The strain dependence of the drain current in a $\mathrm{Si}_{0.75}\mathrm{Ge}_{0.25} - \mathrm{Si}$ HETT was measured, and its dependence was consistent with band-to-band tunneling in the [110] direction. We have derived a new figure of merit $\gamma = (d/d\ln J_D)(d\ln J_D/ds)$ and demonstrated the predicted linear dependence of $d\ln J_D/ds$ on $\ln J_D$. The values of γ of ~ -12 were obtained, which agreed relatively well with theoretical predictions based upon tight-binding band-structure calculations [9]. Ways of using strain to enhance HETT performance were suggested.

REFERENCES

[1] P.-F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weis, D. Schmitt-Landsiedel, and W. Hansch, "Complementary tunneling transistor for low power application," *Solid State Electron.*, vol. 48, no. 12, pp. 2281–2286, Dec. 2004.

[2] C. G. van de Walle and R. M. Martin, "Theoretical calculations of heterojunction discontinuities in the Si/Ge system," *Phys. Rev. B. Condens. Matter*, vol. 34, no. 8, pp. 5621–5634, Oct. 1986.

[3] P.-F. Guo, L.-T. Yang, Y. Yang, L. Fan, G.-Q. Han, G. S. Samudra, and Y.-C. Yeo, "Tunneling field-effect transistor: Effect of strain and temperature on tunneling current," *IEEE Electron Device Lett.*, vol. 30, no. 9, pp. 981–983, Sep. 2009.

[4] T. Krishnamohan, C. Jungemann, K. Donghyun, E. Ungersboeck, S. Selberherr, P. Wong, Y. Nishi, and K. Saraswat, "Theoretical investigation of performance in uniaxially- and biaxially-strained Si, SiGe and Ge double-gate p-MOSFETs," in *IEDM Tech. Dig.*, 2006, pp. 943–946.

[5] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *J. Appl. Phys.*, vol. 80, no. 4, pp. 2234–2252, Aug. 1996.

[6] Sentaurus Device Simulator, Synopsys, Mountain View, CA, 2009. [Online]. Available: http://www.cadfamily.com/download/EDA/sYNOPSYS2008/sdevice_ug.pdf

[7] E. O. Kane, "Theory of tunneling," *J. Appl. Phys.*, vol. 32, no. 1, pp. 83–91, Jan. 1961.

[8] S. E. Laux, "Computation of complex band structures in bulk and confined structures," in *Proc. 13th IWCE*, 2009, pp. 5–8.

[9] M. Luisier, G. Klimeck, A. Schenk, and W. Fichtner, "Atomistic simulation of nanowires in the $sp^3d^5s^*$ tight-binding formalism: From boundary conditions to strain calculations," *Phys. Rev. B*, vol. 74, no. 20, pp. 205 323-1–205 323-12, Nov. 2006.

[10] T. B. Boykin, M. Luisier, M. Salmani-Jelodar, and G. Klimeck, "Strain-induced, off-diagonal, same-atom parameters in empirical tight-binding theory suitable for [110] uniaxial strain applied to a silicon parametrization," *Phys. Rev. B*, vol. 81, no. 12, pp. 125 202-1–125 202-9, Mar. 2010.