Ultrathin Strained-Ge Channel P-MOSFETs With High-K/Metal Gate and Sub-1-nm Equivalent Oxide Thickness

Pouya Hashemi, *Member, IEEE*, Winston Chern, Hyung-Seok Lee, James T. Teherani, Yu Zhu, Jemima Gonsalvez, Ghavam G. Shahidi, *Fellow, IEEE*, and Judy L. Hoyt, *Fellow, IEEE*

***Abstract*—Surface-channel strained-Ge (s-Ge) p-MOSFETs with high-K/metal gate stack and ozone surface passivation are fabricated, for the first time. The channel is ultrathin ($\sim$3–6 nm thick) s-Ge ($\sim$2.2%, biaxial compression) epitaxially grown on a relaxed $Si_{0.56}Ge_{0.44}$ virtual substrate. Split capacitance–voltage measurements along with quantum-mechanical simulations demonstrate a capacitance-equivalent thickness of 1.3 nm and sub-1-nm equivalent oxide thickness. The effective hole mobility of these devices was extracted and exhibits 3$\times$ and 2.2$\times$ mobility enhancement over universal Si hole mobility, for s-Ge channel thicknesses of $\sim$6 and $\sim$3 nm, respectively.**

***Index Terms*—Capacitance-equivalent thickness (CET), high-K, metal gate, mobility, ozone, SiGe, strained Ge (s-Ge).**

I. Introduction

STRAINED-Germanium (s-Ge) channel p-MOSFETs are a promising candidate for future high-performance and low-power-supply-voltage CMOS generations due to their superior mobility and source injection velocity as well as compatibility with Si technology [1]. High hole mobility enhancements over Si have been reported for s-Ge quantum-well p-FETs using Si-cap surface passivation and deposited thick SiO_2 [2]–[5] or high-K/metal gate stack [6]–[10], resulting in relatively high capacitance-equivalent thickness (CET) values. For an s-Ge channel to replace strained Si in future CMOS nodes, sub-1-nm equivalent oxide thickness (EOT) is desirable, which requires the elimination of the strained-Si cap in a surface-channel operation mode. Ritenour *et al.* have reported the mobility of 55-nm-thick s-Ge/$Si_{0.3}Ge_{0.7}$ p-FETs with 1.8-nm EOT and low mobility enhancement over universal or bulk Ge [11]. Recently, sub-1-nm EOT has been demonstrated on relaxed bulk Ge n- and p-FETs using Si monolayer passivation [12], ozone (O_3) surface passivation [13], or plasma postoxidation techniques [14]. However, the hole mobility of s-Ge p-FETs with scaled EOT has not been investigated. In this letter, surface-channel s-Ge p-FETs with an ultrathin (sub-6 nm) channel and very high strain (2.2%) have been fabricated. Using O_3 surface passivation and HK/MG stack technology, sub-1-nm EOT has been demonstrated on s-Ge for the first time. Effective-hole-mobility measurements indicate enhancements as high as 3$\times$ over Si universal hole mobility for such ultrathin layers of s-Ge, and the mobility is sensitive to the channel thickness.

Manuscript received March 20, 2012; accepted April 13, 2012. Date of publication May 24, 2012; date of current version June 22, 2012. This work was supported by the FCRP Center on Materials, Structures, and Devices. The review of this letter was arranged by Editor K.-S. Chang-Liao.

P. Hashemi is with the Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA, and also with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: hashemi@us.ibm.com).

W. Chern, H.-S. Lee, J. T. Teherani, and J. L. Hoyt are with the Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

Y. Zhu, J. Gonsalvez, and G. G. Shahidi are with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2012.2195631

II. Device Design and Fabrication

The fabrication process starts with the epitaxial growth of a heterostructure of s-Ge/relaxed $Si_{1-x}Ge_x$ $(x = 0.44)$/$Si_{1-y}Ge_y$ ($y = 0$ to 0.44) graded buffer on N^+-doped Si wafers, in an AMAT Epi Centura reactor. Relaxed SiGe layers were *in situ* doped (n-type) to a level of 10^{17} cm^{-3}. The s-Ge was grown at 365 °C, and X-ray diffraction analysis on similarly grown samples shows that the Ge is fully strained to the relaxed SiGe layer. Following heteroepitaxy, the wafers were immediately capped with low-temperature oxide (LTO). Active areas were partially opened by lithography-defined dry etching, and the wafers were cleaned in 4:1 $H_2SO_4 : H_2O_2$ while the last 30-nm LTO was opened in 50:1 H_2O:HF. The wafers were then immediately subjected to O_3 surface passivation at 200 °C, followed by *in situ* HfO_2 (45 cycles at 200 °C)/WN (1000 cycles at 340 °C) HK/MG stack, all in an atomic layer deposition (ALD) system, similar to the process in [13]. Long-channel ($L = 5$ and 50 μm) p-FETs were fabricated using a square-ring FET layout, with sides parallel to the $\langle 110 \rangle$ directions. After the gate dry etch, the S/D regions were implanted with boron that was activated at a temperature of 500 °C in N_2. The fabrication was completed by metallization and a forming gas anneal at 450 °C. Effective hole mobility was extracted using split-CV and low-V_{DS} drain current measurements on 50-μm-channel-length ring FETs. Layer thicknesses were measured using cross-sectional TEM (XTEM) and ellipsometry. About 5 nm of s-Ge thickness loss was measured due to the device processing. The Ge content of the relaxed buffer layer ($x = 43.6\%$) was measured using SIMS, resulting in around 2.2% biaxial compression in the channel, assuming that the Ge film is pseudomorphically strained with respect to a fully relaxed $Si_{0.56}Ge_{0.44}$ layer.

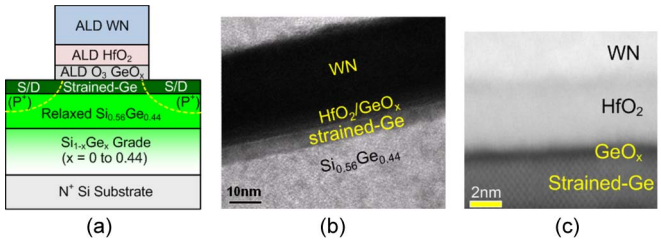

Fig. 1. (a) Structural schematic and corresponding cross-sectional (b) TEM and (c) high-resolution STEM images of the fabricated ultrathin s-Ge channel p-FETs with $GeO_x/HfO_2/WN$ gate stack.

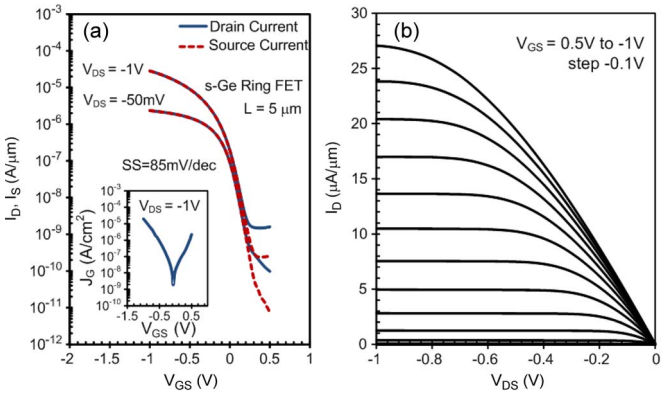

Fig. 2. Typical (a) transfer and (b) output characteristics of ∼6-nm-thick s-Ge channel ring p-FETs ($L = 5\ \mu$m) with $GeO_x/HfO_2/WN$ gate stack. The inset of (a) shows the typical gate leakage characteristics.

III. Results and Discussion

Fig. 1(a) illustrates the cross-sectional schematic of the fabricated p-FETs with $GeO_x/HfO_2/WN$ gate stack. The XTEM shown in Fig. 1(b) demonstrates a device with a 6-nm s-Ge, 4-nm HfO_2, and 30-nm WN. Fig. 1(c) shows the high-resolution STEM image of the s-Ge device, indicating ∼6-Å GeO_x due to O_3 surface treatment. The typical transfer and output characteristics of the ∼6-nm-thick s-Ge ring FETs ($L = 5\ \mu$m) are shown in Fig. 2. Devices show a subthreshold slope (SS) of 85 mV/dec over three decades and more than four orders of magnitude on/off ratio, among the best reports for s-Ge p-FETs to date [3]–[12]. Moreover, the inset of Fig. 2(a) shows the typical gate leakage density (J_G) measured at $V_{DS} = -1$ V, showing $J_G = 2 \times 10^{-5}$ A · cm^{-2} at $V_{GS} = -1$ V.

Fig. 3(a) shows the measured gate-channel capacitance of s-Ge (6-nm thick) p-FETs at $f = 1$ MHz, using split capacitance–voltage (C–V) technique. In addition, Fig. 3(b) shows the corresponding hysteresis and frequency-dispersion ($f = 10$ kHz−1 MHz) characteristics of the s-Ge devices, showing reasonable hysteresis (less than 60 mV at 1 MHz) and frequency dispersion. A CET of 1.3 nm was measured at $V_{GS} = -1$ V. Using the conductance method, midgap D_{it} of $\sim 3 \times 10^{12}$ cm^{-2} · eV^{-1} was measured which is consistent with the extracted value based on the SS. To extract the EOT for such a heterostructure, 1-D simulations using nextnano^3 [15] were performed, using full-band quasistatic quantum-mechanical simulations with a $6 \times 6\ k \cdot p$ quantization method for the Ge valence band and a constant 10^{17}-cm^{-3} n-type doping throughout the structure. The simulated results for EOT = 9, 10, and 11 Å are overlaid in Fig. 3(a). As the measured results fall between an EOT of 9 and 10 Å, sub-1-nm EOT has been achieved for s-Ge MOSFETs, for the first time.

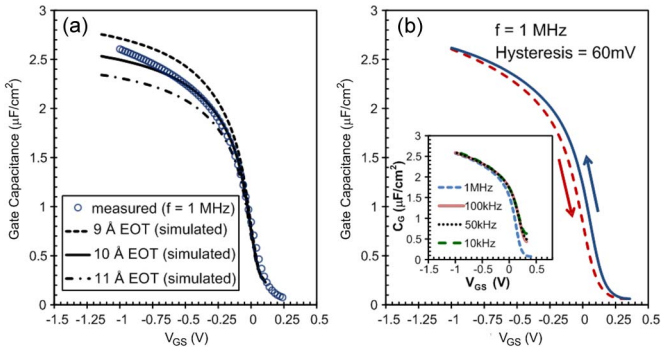

Fig. 3. (a) Measured gate-channel C–V characteristics of s-Ge channel p-FETs; Overlaid are QM simulated C–V curves for EOT = 9, 10, and 11 Å, demonstrating sub-1-nm EOT. (b) Hysteresis and frequency-dispersion C–V characteristics of s-Ge p-FETs with XTEM shown in Fig. 1(b).

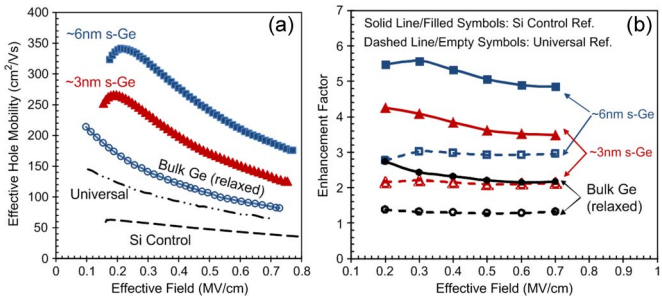

Fig. 4. (a) Effective hole mobility of ∼6- and ∼3-nm s-Ge channel p-FETs with HK/MG stack versus effective field. Overlaid are universal hole mobility, mobility of processed Si control, and bulk relaxed Ge [13] with O_3 surface passivation and HfO_2/WN gate stack. (b) Corresponding mobility enhancement factor versus effective field over the (dashed line/empty symbols) universal and (solid line/field symbols) Si control.

The effective-hole-mobility characteristics of s-Ge p-MOSFETs with s-Ge thicknesses of ∼6 and ∼3 nm versus effective field are shown in Fig. 4(a). Overlaid are universal hole mobility, mobility of processed Si control, and bulk relaxed Ge [13] with O_3 surface passivation and HfO_2/WN gate stack. The deterioration in the low-field (< 0.2 MV/cm) mobility for the s-Ge is due to the relatively high D_{it}. Fig. 4(b) shows the hole mobility enhancement factor over the universal and Si control sample for ultrathin s-Ge channels with CET = 1.3 nm, as well as bulk Ge (relaxed) p-FETs. Mobility enhancement factors of 3× over hole universal and more than 5× over control Si are observed for ∼6-nm-thick s-Ge channels at CET = 1.3 nm. The hole mobility drops for the ∼3-nm-thick channel, compared to ∼6 nm, due to the increased quantum-mechanical confinement as the width of the quantum well is decreased, consistent with observations on SiGe-channel p-MOSFETs [16].

IV. Summary and Conclusion

In summary, surface-channel highly strained (2.2% biaxial compression) Ge/relaxed $Si_{0.56}Ge_{0.44}$ p-MOSFETs featuring sub-1-nm EOT have been fabricated and characterized, for the first time. ALD O_3 surface passivation prior to high-K/metal gate stack deposition has been performed to form ∼6-Å GeO_x interface between s-Ge and HfO_2. The fabricated devices have exhibited reasonable transfer, output, and gate leakage characteristics. C–V measurements along with quantum-mechanical simulations have demonstrated a CET of 1.3 nm and sub-1-nm

EOT, with moderate frequency dispersion and hysteresis. The effective hole mobility of MOSFETs with ∼3- and ∼6-nm s-Ge channel thicknesses was extracted, demonstrating 3× and 2.2× mobility enhancements over the hole universal curve and approximately 5× and 4× over control Si devices, for ∼6- and ∼3-nm-thick s-Ge, respectively. The results with scaled EOT indicate that s-Ge p-FETs are promising candidates for future high-performance low-power-supply-voltage CMOS generations.

ACKNOWLEDGMENT

The authors would like to thank G. Riggott, J. Hennessey, D. A. Antoniadis, and the MIT Microsystems Technology Laboratories staff for helpful discussions.

REFERENCES

[1] F. Conzatti, P. Toniutti, D. Esseni, P. Palestri, and L. Selmi, "Simulation study of the on-current improvements in Ge and s-Ge versus Si and s-Si nano-MOSFETs," in *IEDM Tech. Dig.*, 2010, pp. 15.2.1–15.2.4.

[2] M. L. Lee and E. A. Fitzgerald, "Optimized strained Si/strained Ge dual channel heterostructures for high mobility p- and n-MOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 18.1.1–18.1.4.

[3] C. Ni Chléirigh, "Strained SiGe-channel p-MOSFETs: Impact of heterostructure design and process technology," Ph.D. thesis, Massachusetts Inst. Technol., Cambridge, MA, 2007.

[4] T. Krishnamohan, Z. Krivokapic, K. Uchida, Y. Nishi, and K. C. Saraswat, "High-mobility ultrathin strained Ge MOSFETs on bulk and SOI with low band-to-band tunneling leakage: Experiments," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 990–999, May 2006.

[5] H. Shang, J. O. Chu, S. Bedell, E. P. Gusev, P. Jamison, Y. Zhang, J. A. Ott, M. Copel, D. Sadana, K. W. Guarini, and M. Ieong, "Selectively formed high mobility strained Ge PMOSFETs for high performance CMOS," in *IEDM Tech. Dig.*, 2004, pp. 157–160.

[6] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L.-Â Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," in *IEDM Tech. Dig.*, 2006, pp. 1–4.

[7] G. Nicholas, T. J. Grasby, D. J. F. Fulgoni, C. S. Beer, J. Parsons, M. Meuris, and M. M. Heyns, "High mobility strained Ge pMOSFETs with high-κ/metal gate," *IEEE Electron Device Lett.*, vol. 28, no. 9, pp. 825–827, Sep. 2007.

[8] O. Weber, Y. Bogumilowicz, T. Ernst, J.-M. Hartmann, F. Ducroquet, F. Andrieu, C. Dupre, L. Clavelier, C. Le Royer, N. Cherkashin, M. Hytch, D. Rouchon, H. Dansas, A.-M. Papon, V. Carron, C. Tabone, and S. Deleonibus, "Strained Si and Ge with high-κ/metal gate stack for high mobility dual channel CMOS," in *IEDM Tech. Dig.*, 2005, pp. 137–140.

[9] R. Pillarisetty, B. Chu-Kung, S. Corcoran, G. Dewey, J. Kavalieros, H. Kennel, R. Kotlyar, V. Le, D. Lionberger, M. Metz, N. Mukherjee, J. Nah, W. Rachmady, M. Radosavljevic, U. Shah, S. Taft, H. Then, N. Zelick, and R. Chau, "High mobility strained Ge quantum well field effect transistor as the P-channel device option for low power ($V_{cc} = 0.5$ V) III-V CMOS Architecture," in *IEDM Tech. Dig.*, 2010, pp. 6.7.1–6.7.4.

[10] P. Hashemi and J. L. Hoyt, "High hole-mobility strained-Ge/$Si_{0.6}Ge_{0.4}$ p-MOSFETs with high-κ/metal gate: Role of strained-Si cap thickness," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 173–175, Feb. 2012.

[11] A. Ritenour, S. Yu, M. L. Lee, N. Lu, W. Bai, A. Pitera, E. A. Fitzgerald, D. L. Kwong, and D. A. Antoniadis, "Epitaxial strained germanium p-MOSFETs with HfO_2 gate dielectric and TaN gate electrode," in *IEDM Tech. Dig.*, 2003, pp. 18.2.1–18.2.4.

[12] J. Mitard, C. Shea, B. De Jaeger, A. Pristera, G. Wang, M. Houssa, G. Eneman, G. Hellings, W.-E. Wang, J. C. Lin, F. E. Leys, R. Loo, G. Winderickx, E. Vrancken, A. Stesmans, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M. M. Heyns, "Impact of EOT scaling down to 0.85 nm on 70-nm Ge-p-FETs technology with STI," in *VLSI Symp. Tech. Dig.*, 2009, pp. 82–83.

[13] J. Hennessy and D. A. Antoniadis, "High electron mobility germanium MOSFETs: Effect of n-type channel implants and ozone surface passivation," in *Proc. Device Res. Conf. Tech. Dig.*, 2009, pp. 257–258.

[14] R. Zhang, N. Taoka, P.-C. Huang, M. Takenaka, and S. Takagi, "1-nm-thick EOT high mobility Ge n- and p-MOSFETs with ultrathin GeO_x/Ge MOS interfaces fabricated by plasma post oxidation," in *IEDM Tech. Dig.*, 2011, pp. 28.3.1–28.3.4.

[15] $nextnano^3$. [Online]. Available: http://www.nextnano.de

[16] C. Ni Chleirigh, N. D. Theodore, H. Fukuyama, S. Mure, H.-U. Ehrke, A. Domenicucci, and J. L. Hoyt, "Thickness dependence of hole mobility in ultrathin SiGe-channel p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2687–2694, Oct. 2008.