# Record Hole Mobility at High Vertical Fields in Planar Strained Germanium on Insulator With Asymmetric Strain

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***Abstract*— Long channel asymmetrically strained Ge narrow width p-MOSFETs were fabricated from (100) biaxially strained Ge (strain ∼ 2.5%) on insulator. Devices with widths of 0.425–15 μm were fabricated with <110> and <100> channel directions. Reducing the mesa width caused mobility to increase for <110> but decrease for <100> channel orientations. The highest mobility was observed for 0.425-μm-wide mesas with <110> channel direction with an enhancement of 45%–50% relative to biaxially strained Ge at $N_{\text{inv}} = 6 \times 10^{12}$ cm$^{-2}$ and a record mobility of 955 cm$^2$/Vs at $N_{\text{inv}} = 10^{13}$ cm$^{-2}$. Mesas up to 2-μm wide were observed to have enhanced mobilities relative to biaxial Ge, suggesting that even relatively wide mesas can be affected by patterning-induced strain relaxation.**

***Index Terms*— Strained-Ge, high-κ, metal gate, SiGe, mobility, narrow width, asymmetric, heterostructure, thin-body, strain.**

## I. Introduction

HIGH mobility channel materials, such as Ge and III-Vs, are being explored to improve the current drive for continued performance scaling of CMOS transistors [1]–[3]. Strained-Ge (s-Ge) p-MOSFETs are of interest because of their superior transport characteristics and compatibility with Si technology [4], [5]. High hole mobilities have been demonstrated in combination with high-κ/metal gate technology for Si-capped biaxially s-Ge [6]–[10]. Further improvements in the mobility of s-Ge have been demonstrated through recently fabricated uniaxially [11], [12] and asymmetrically [13] s-Ge nanowires.

In this letter we demonstrate mobility enhancement from the narrow width effect or lateral strain relaxation generated from lithographic patterning of initially biaxial s-Ge with 2.5% compressive strain. The lateral component of the biaxial strain relaxes due to the free surfaces generated when patterning narrow mesas resulting in asymmetric strain [13]–[19]. The improvement of the mobility is analyzed as a function of mesa width and channel direction. A record high hole mobility for all p-type materials is demonstrated at $N_{\text{inv}} = 10^{13}$ cm$^{-2}$.

Manuscript received December 23, 2013; accepted January 7, 2014. Date of publication January 10, 2014; date of current version February 20, 2014. This work was supported by the FCRP Center on Materials, Structures, and Devices. The review of this letter was arranged by Editor J. Schmitz.

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Digital Object Identifier 10.1109/LED.2014.2300197

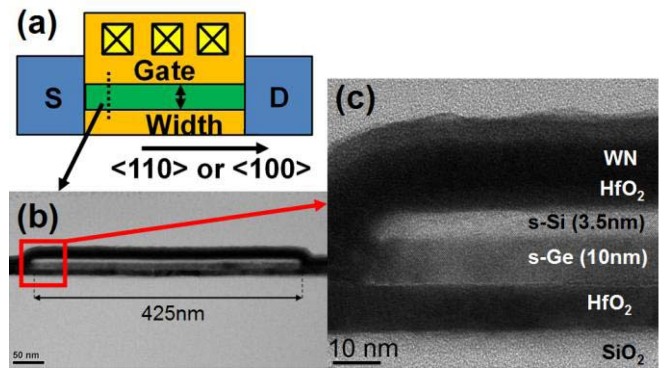


Fig. 1. (a) Top-down schematic of s-Ge narrow width p-MOSFETs. (b) XTEM of the channel of a nominally 500 nm wide device showing a 75 nm correction to the nominal mesa width. (c) High resolution XTEM showing the channel heterostructure of 3.5 nm s-Si/10 nm s-Ge.

## II. Device Design and Fabrication

SGDOI (s-Ge directly on insulator) wafers were fabricated using a bond and etch-back technique similar to [20] with relaxed $Si_{0.6}Ge_{0.4}$ as the donor virtual substrate. The resulting magnitude of biaxial strain in the Ge layer is 2.5%. The substrate consists of 5 nm s-Si/10 nm s-Ge on a 10 nm $HfO_2$/440 nm $SiO_2$ buried oxide layer. The (100) SGDOI substrate was patterned using photolithography to form the narrow width device structure in the <100> and <110> orientations [Fig. 1(a)]; (110) wafers would yield higher mobilities although our current materials technology is calibrated for (100). *In-situ* $O_3$ pretreatment was performed prior to the ALD deposition of 40Å $HfO_2$ gate dielectric and a WN gate. The source/drain implant was 5 keV, $2\times10^{15}$ cm$^{-2}$ boron. A 500 °C, 30 min. post-implant anneal activated the dopants and a standard ILD, Al/Ti metallization process followed. The XTEM of the device shows the actual mesa width for a nominally W = 500 nm, <110> oriented mesa [Fig. 1(b)]; XTEM was used to correct the mesa width. The final thicknesses measured by XTEM are 3.5-nm s-Si/10-nm s-Ge [Fig. 1(c)].

## III. Results and Discussion

The linear transfer characteristics [Fig. 2(a)] show an increase in $I_D$ lin. for decreasing mesa width. The C-V characteristics [Fig. 2(b)] show that the capacitance scales fairly well with mesa area suggesting the mechanism for

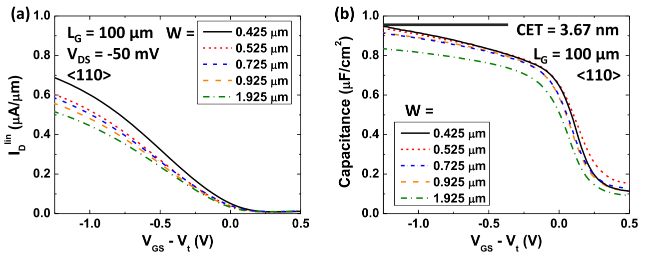


Fig. 2. Normalized (a) linear transfer and (b) C-V characteristics for <110> oriented narrow width devices. The normalization was done using $W_{eff} = W + 2H_{mesa}$ where W is the width based upon the XTEM and $H_{mesa}$ is the height of the mesa.

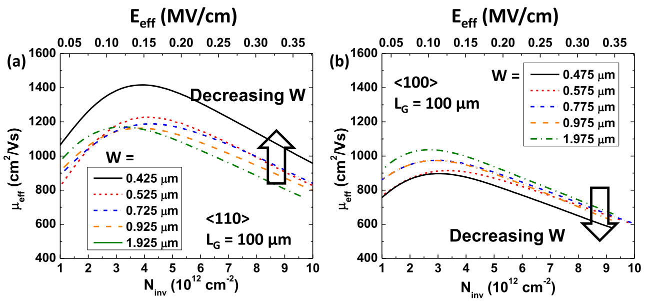


Fig. 3. Extracted $\mu_{eff}$ vs. $N_{inv}$ for (a) <110> and (b) <110> oriented devices for nominally W = 425 nm to ∼2 $\mu$m; $N_{inv}$ was derived using $W_{eff}$. The general trend is the mobility increases for <110> and decreases for <100> for decreasing mesa width.

enhanced $I_D$ lin. is mobility enhancement. The mobility was extracted for mesas of various widths and channel orientations using the split-CV method (Fig. 3). For the <110> orientation, mobility is observed to be increasing with decreasing width while the opposite trend is true for the <100> direction. Devices in the <100> direction will have degraded performance in asymmetrically or uniaxially strained Ge p-MOSFETs [21], [22]. The discrepancy in the trends for different orientations is not only due to the transport direction, but the impact of the direction of strain relaxation on the valence band structure [21], [22]. For the <110> and <100> oriented devices, strain relaxation occurs in the <110> and <100> directions respectively. The combination of both of these properties causes the mobility to diverge with increasing strain relaxation as the mesa width decreases (Fig. 4). The increase in mobility for the <110> direction can be observed all the way to the narrow nanowire regime previously published in [13]. The smallest mesa with W = 425 nm has a 45-50% increase in mobility relative to biaxial at $N_{inv} = 6\times10^{12}$ cm$^{-2}$. Even at large widths, W ∼ 2 $\mu$m, there is a large discrepancy (∼20%) in the mobility for the different channel directions. For mesas with W = 15 $\mu$m, there was no mobility dependence upon channel orientation indicating that the strain is biaxial. In order to understand the mobility enhancement, strain simulations were performed in COMSOL [23]. The lateral strain at the center of the mesa for W = 400 nm and 2 $\mu$m was −2.25% and −2.43% respectively for an initially −2.5% biaxially-strained film. The strain is slightly asymmetric in the center of the mesa. Based upon the magnitude of the strain asymmetry at the center of the mesa and ref. 24, for a mesa with W = 2 $\mu$m

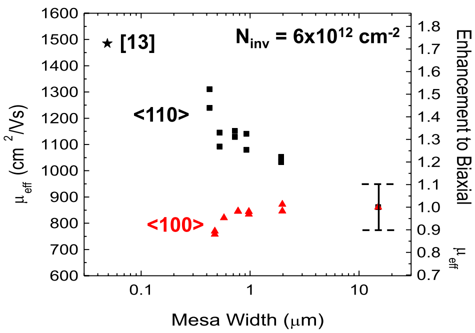


Fig. 4. $\mu_{eff}$ vs. mesa width by split-CV method for <110> and <110> channel orientations for $N_{inv} = 6\times10^{12}$ cm$^{-2}$. The $\mu_{eff}$ for biaxially strained s-Ge is estimated for W = 15 $\mu$m using $Q_{inv} = q * C_{ox} * (V_{GS} - V_t)$. The error bar represents a +/ − 10% $\mu_{eff}$ error due to that estimate. Also shown is the $W_{NW}$ = 49 nm trigate p-MOSFET in [13] to show the effect of further lateral strain relaxation.

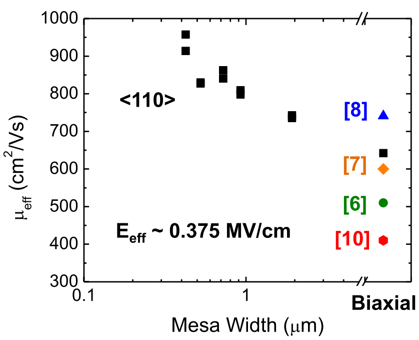


Fig. 5. $\mu_{eff}$ vs. mesa width for <110> channel orientation at $E_{eff}$ = 0.375 MV/cm (this is the equivalent of $N_{inv} = 10^{13}$ cm$^{-2}$ for the devices in this work). The narrow width devices are benchmarked against previously reported high-$\kappa$/metal gate s-Si capped s-Ge devices at equivalent $E_{eff}$ [6]–[8], [10].

one would expect a 10% mobility increase. This prediction is in-line with our observed mobility improvement because additional strain relaxation occurs near the edge of the mesa.

The mobilities for the narrow width devices were also compared to literature values for high-$\kappa$/s-Si capped s-Ge (Fig. 5) at $E_{eff}$ ∼ 0.375 MV/cm – equivalent to $N_{inv} = 10^{13}$ cm$^{-2}$ for the narrow width devices [6]–[8], [10]. The narrowest width devices, W = 425 nm, have a mobility enhancement of ∼25% relative to the highest biaxially s-Ge mobility reported to date [8] due to the lateral strain relaxation.

## IV. Conclusion

In summary, mobility was extracted from long channel, narrow width devices fabricated on biaxial SGDOI wafers. The mobility showed orientation dependence due to both the channel direction and strain relaxation. The <100> and <110> oriented devices showed reduced and enhanced mobility with decreasing mesa width respectively. At $N_{inv}$ = $6\times10^{12}$ cm$^{-2}$, the narrowest <110> devices showed 45-50% mobility improvement relative to biaxially s-Ge and a record $\mu_{eff}$ = 955 cm$^2$/Vs at $E_{eff}$ = 0.375 MV/cm ($N_{inv}$ = $10^{13}$ cm$^{-2}$) due to the asymmetric strain caused by the lateral relaxation of the mesa.

## Acknowledgment

The authors thank G. Riggott, J. Ott, G. Shahidi, T. Yu, and the MIT Microsystems Technology Laboratories staff for helpful discussions.

## References

[1] A. Khakifirooz and D. A. Antoniadis, "Transistor performance scaling: The role of virtual source velocity and its mobility dependence," in *Proc. IEDM*, Dec. 2006, pp. 667–670.

[2] R. Pillarisetty, "Academic and industry research progress in germanium nanodevices," *Nature*, vol. 479, no. 7373, pp. 324–328, Nov. 2011.

[3] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, Nov. 2011.

[4] F. Conzatti, P. Toniutti, D. Esseni, *et al.*, "Simulation study of the on-current improvements in Ge and s-Ge versus Si and s-Si nano-MOSFETs," in *Proc. IEEE IEDM*, Dec. 2010, pp. 363–366.

[5] S. W. Bedell, A. Majumdar, J. A. Ott, *et al.*, "Mobility scaling in short-channel length strained Ge-on-insulator P-MOSFETs," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 811–813, Jul. 2008.

[6] O. Weber, Y. Bogumilowicz, T. Ernst, *et al.*, "Strained Si and Ge with high-k/metal gate stack for high mobility dual channel CMOS," in *Proc. IEEE IEDM*, Dec. 2005, pp. 137–140.

[7] R. Pillarisetty, B. Chu-Kung, S. Corcoran, *et al.*, "High mobility strained Ge quantum well field effect transistor as the p-channel device option for low power (Vcc= 0.5V) III–V CMOS architecture," in *Proc. IEEE IEDM*, Dec. 2010, pp. 150–153.

[8] P. Hashemi and J. L. Hoyt, "High hole-mobility strained-Ge/$Si_{0.6}$ $Ge_{0.4}$ p-MOSFETs with high-K/metal gate: Role of strained-Si cap thickness," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 173–175, Feb. 2012.

[9] C. Ni Chléirigh, "Strained SiGe-channel p-MOSFETs: Impact of heterostructure design and process technology," Ph.D. dissertation, MIT, Cambridge, MA, USA, 2007.

[10] G. Nicholas, T. J. Grasby, D. J. F. Fulgoni, *et al.*, "High mobility strained Ge pMOSFETs with High-$\kappa$/metal gate," *IEEE Electron Device Lett.*, vol. 28, no. 9, pp. 825–827, Sep. 2007.

[11] K. Ikeda, M. Ono, D. Kosemura, *et al.*, "High-mobility and low-parasitic resistance characteristics in strained Ge nanowire pMOSFETs with metal source/drain structure formed by doping-free processes," in *Proc. Symp. VLSI Technol.*, Jun. 2012, pp. 165–166.

[12] K. Ikeda, Y. Kamimuta, Y. Moriyama, *et al.*, "Enhancement of hole mobility and cut-off characteristics of strained Ge nanowire pMOSFETs by using plasma oxidized GeOx inter-layer for gate stack," in *Proc. Symp. VLSI Technol.*, Jun. 2013, pp. T30–T31.

[13] W. Chern, P. Hashemi, J. T. Teherani, *et al.*, "High mobility high-$\kappa$-all-around asymmetrically-strained germanium nanowire trigate p-MOSFETs," in *Proc. IEEE IEDM*, Dec. 2012, pp. 387–390.

[14] P. Hashemi, L. Gomez, J. L. Hoyt, *et al.*, "Asymmetric strain in nanoscale patterned strained-Si/strained-Ge/strained-Si heterostructures on insulator," *Appl. Phys. Lett.*, vol. 91, no. 8, pp. 083109-1–083109-3, Aug. 2007.

[15] S. W. Bedell, N. Daval, A. Khakifirooz, *et al.*, "New opportunities for SiGe and Ge channel p-FETs," *Microelectron. Eng.*, vol. 88, no. 4, pp. 324–330, Apr. 2011.

[16] T. Irisawa, T. Numata, T. Tezuka, *et al.*, "High-performance uniaxially strained SiGe-on-insulator pMOSFETs fabricated by lateral-strain-relaxation technique," *IEEE Trans. Electron. Devices*, vol. 53, no. 11, pp. 2809–2815, Nov. 2006.

[17] K. Cheng, A. Khakifirooz, N. Loubet, *et al.*, "High performance extremely thin SOI (ETSOI) hybrid CMOS with Si channel NFET and strained SiGe channel PFET," in *Proc. IEEE IEDM*, Dec. 2012, pp. 419–422.

[18] J. Mitard, L. Witters, B. Vincent, *et al.*, "First demonstration of strained Ge-in-STI IFWQ pFETs featuring raised SiGe75% S/D, replacement metal gate and germanided local interconnects," in *Proc. Symp. VLSIC*, Jun. 2013, pp. T20–T21.

[19] P. Hashemi, *et al.*, "High-performance Si1-xGex channel on insulator trigate PFETs featuring an implant-free process and aggressively-scaled fin and gate dimensions," in *Proc. Symp. VLSIC*, Jun. 2013, T18–T19.

[20] L. Gomez, M. Canonico, M. K. Kim, *et al.*, "Fabrication of strained-Si/strained-Ge heterostructures on insulator," *J. Electron. Mater.*, vol. 37, no. 3, pp. 240–244, Mar. 2008.

[21] C. Y. Kang, R. Choi, S. C. Song, *et al.*, "A novel electrode-induced strain engineering for high performance SOI FinFET utilizing Si (110) channel for both N and PMOSFETS," in *Proc. IEDM*, Dec. 2006, pp. 885–888.

[22] T. Krishnamohan, D. Kim, T. V. Dinh, *et al.*, "Comparison of (001), (110) and (111) uniaxial- and biaxial- strained-Ge and strained-Si PMOS DGFETs for all channel orientations: Mobility enhancement, drive current, delay and off-state leakage," in *Proc. IEEE IEDM*, Dec. 2008, pp. 899–902.

[23] *COMSOL Multiphysics* [Online]. Available: http://www.comsol.com/

[24] L. Gomez, C. Ni Chléirigh, P. Hashemi, *et al.*, "Enhanced hole mobility in high Ge content asymmetrically strained-SiGe p-MOSFETs," *IEEE Electron Device Letters*, vol. 31, no. 8, pp. 782–784, Aug. 2010.