High Mobility High-κ-All-Around Asymmetrically-Strained Germanium Nanowire Trigate p-MOSFETs

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Abstract

We demonstrate for the first time, asymmetrically strained Ge, high-κ/metal gate nanowire (NW) trigate p-MOSFETs with record hole mobility of 1490 cm^2/Vs. This mobility is 2× above on-chip, biaxially strained Ge planar FETs and ~15× above Si universal mobility. The fabrication approach features: (1) a new strained Si/strained Ge/HfO_2 NW channel materials stack, with HfO_2 dielectric at the bottom which acts as an excellent etch stop for top-down NW formation, and also unpins the back Ge-dielectric interface, (2) large compressive biaxial strain (~2.5%) that is built into the channel material prior to layer transfer, and (3) lateral strain relaxation by nanoscale patterning of the channel. The resulting *asymmetric* strain distribution dramatically reduces the conductivity effective mass. 6×6 k.p quantum mechanical simulations predict an increase in the Ge NW average inverse effective mass by a factor of 1.6 relative to planar biaxially strained Ge, consistent with the measured 2× mobility enhancement.

Introduction

The investigation of MOSFETs utilizing channel materials with enhanced transport, in device architectures that offer improved scalability, is critical for future logic technology. Ge has very high hole mobility, which makes it attractive for enhancing p-MOSFET current drive, especially for low voltage applications. Extremely high hole mobility (~1000 cm^2/Vs) has been reported in planar high-κ/metal gate MOSFETs with Ge channels under biaxial compression (1,2). Recently, strained Ge NW, metal S/D p-MOSFETs with nanowire width W_{NW} = 20 nm, formed using a Ge condensation technique, with a peak mobility of 855 cm^2/Vs have been reported (3). Here, we demonstrate long channel strained Ge, high-κ-all-around NW trigate p-MOSFETs with record hole mobility of 1490 cm^2/Vs for W_{NW}=49 nm. For W_{NW}=18 nm a mobility of 850 cm^2/Vs is achieved, with $I_{max}/I_{min} > 10^4$, and SS=85 mV/dec., among the best reported for strained Ge channel MOSFETs.

Device Fabrication and Characterization

Fig. 1 shows a schematic of the bond and etch-back process used to fabricate the starting substrates (4). The Ge (and Si cap) is biaxially strained to the relaxed SiGe (~40% Ge) buffer layer, and the strain is maintained during the layer transfer process. The strained Ge-on-insulator is patterned into nanowires by e-beam lithography (EBL) resulting in relaxation of the transverse strain, ε_x, while the strain in the channel direction, ε_z is maintained (Fig. 2) (5). Strain calculations were performed using the *nextnano*[3] simulator (6). The simulated transverse strain is relaxed at the (110) sidewalls for all W_{NW}, is non-uniform in the transverse direction and is asymmetric, i.e. $|\varepsilon_x| < |\varepsilon_z|$ (Fig. 3 and 4). Average transverse strain for various W_{NW} obtained from measured Raman peak shifts relative to unstrained Ge are in good agreement with the simulations, confirming the calculated strain profile dependence on W_{NW} (Fig. 5).

Asymmetrically-strained Ge nanowire trigate p-MOSFETs with W_{NW}= 18 to 50 nm were fabricated using hybrid EBL and photolithography (Fig. 6). On-chip planar (biaxially strained) devices are also included. Devices feature 4 nm of

HfO_2 gate dielectric, a WN metal gate, and have 500 wires in parallel for accurate mobility extraction. A cross-section TEM looking down the [110] channel direction is shown in Fig. 7. The transfer (Fig. 8) and output (Fig. 9) characteristics of the L_g=10 μm, W_{NW}=18 nm device show excellent SS=85 mV/dec., and $I_{max}/I_{min}>10^4$. The relatively constant SS for narrow W_{NW} (Fig. 10) and improvement over the planar FETs is due to the excellent electrostatic control afforded by the sidewall gates. The V_{th} shift with W_{NW} may be caused by a modest level of density of interface states (D_{it}) at the Ge/HfO_2 interfaces. Split-CV (Fig. 11 and 12) displays little frequency dispersion in inversion, and a frequency of 500 kHz was used for accurate mobility extraction.

Results and Discussion

The extracted mobility for all Ge devices shows a significant increase relative to silicon hole universal (Fig. 13). Without a series resistance correction, the mobility of nanowires with $W_{NW}>18$ nm is enhanced with respect to biaxially strained on-chip planar Ge FETs (1.8× for W_{NW}=49 nm at $N_{inv}=7x10^{12}$ cm^{-2}). The series resistance was extracted and results in a small (~10%) increase to the extracted mobilities (Fig. 14). For the W_{NW}=49 nm Ge device, an enhancement of 2× is observed relative to the biaxially strained FET, and ~15× compared to relaxed-Si hole universal at $N_{inv}=7x10^{12}$ cm^{-2}. The measured NW mobility decreases with decreasing W_{NW}, towards the biaxial mobility. To better understand this trend, self-consistent Poisson-Schrödinger simulations were performed to calculate carrier density profiles (Fig. 15). The charge density peaks near the sidewall of the wires where scattering from interface charges and line edge roughness is expected to be significant (~1.2 nm RMS roughness was extracted from SEM images taken during NW processing). The scattering is expected to affect narrower wires more than wider ones because more carriers reside at the device sidewalls (~80% of the integrated charge is within 5 nm of the sidewall for W_{NW}=18 nm *vs*. ~50% for W_{NW}=49 nm).

The average inverse effective mass in the channel direction $\langle\langle 1/m_z \rangle\rangle$ was calculated as shown in Fig. 16. The asymmetrically strained nanowires with (110) sidewalls are predicted to have an increased average inverse effective mass, $\langle\langle 1/m_z \rangle\rangle$ with an increase by a factor of 1.6× for W_{NW}=49 nm relative to the biaxial case, in good agreement with the measured mobility ratio. A small increase in $\langle\langle 1/m_z \rangle\rangle$ with decreasing W_{NW} is also predicted, which bodes well for short channel p-MOSFETs with narrow NWs fabricated with reduced sidewall roughness.

Summary and Conclusion

In summary, asymmetrically strained Ge nanowire trigate p-MOSFETs were fabricated using a high-κ all-around process for the first time, and record hole mobility is demonstrated. A 2× mobility increase is measured for [110] oriented, asymmetrically strained Ge trigates relative to on-chip biaxially strained devices and published mobilities for planar (1) and non-planar Ge FETs (3,11) (Fig. 17). Quantum mechanical simulations predict an average inverse effective mass increase in good agreement with the measured NW-to-biaxial mobility ratio. The results obtained for asymmetrically strained Ge are promising for future high performance CMOS applications.

Acknowledgment

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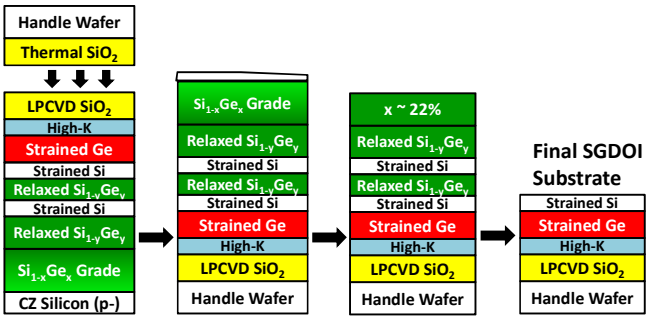

Fig. 1: Schematic of bond and etch-back process to form Strained Ge Directly on Insulator (SGDOI). 10 nm-thick strained-Ge is grown pseudomorphic to a relaxed x=40% $Si_{1-x}Ge_x$ layer. After bonding, all layers except the s-Si/s-Ge are removed. The bottom HfO_2 acts as an etch stop during nanowire formation and can passivate the back Ge-dielectric interface.

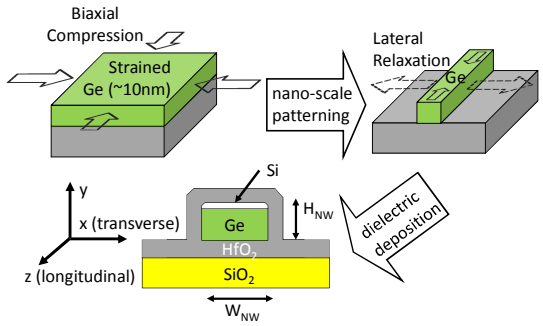

Fig. 2: Schematic of nanowire formation. The biaxially strained SGDOI substrate is patterned to form nanowires. This relaxes the strain in the transverse (x) direction, while maintaining the longitudinal strain in the channel (z) direction. After patterning, HfO_2 is deposited by ALD to form a high-k-all-around structure.

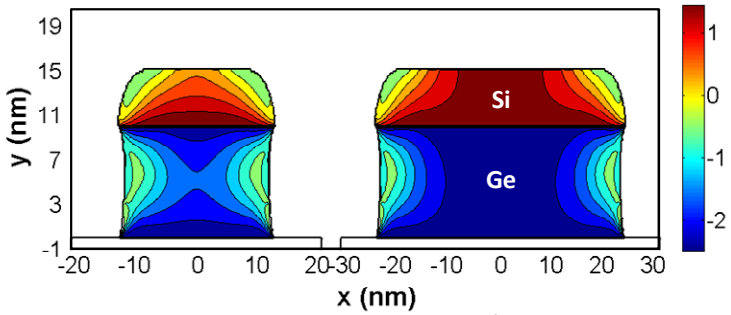

Fig. 3: Simulated transverse strain (ε_x) profiles (nextnano^3 (6)) for nanowires with W_{NW}=26nm and 49nm respectively; color scale is in % strain. Near the sidewalls, the strain in the x-direction is relaxed from the initial value of -2.4%, derived from Ge grown on a 40% SiGe relaxed buffer layer.

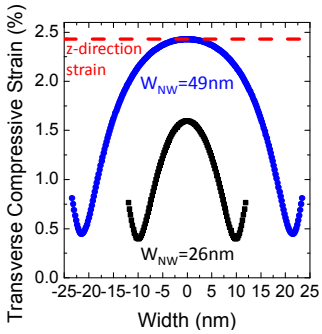

Fig. 4: Transverse strain (ε_x) profiles at y=5nm for W_{NW}= 26 and 49nm. The longitudinal strain (ε_z) is maintained for both cases. The strain is non-uniform and asymmetric ($\varepsilon_x \neq \varepsilon_z$) for both cases.

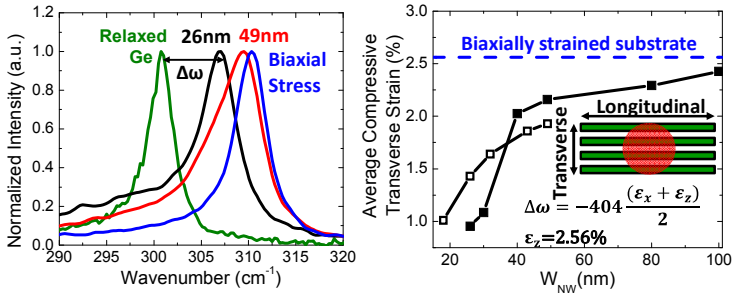

Fig. 5: (left) Measured Raman spectra for relaxed Ge, starting SGDOI, and W_{NW}=26 and 49nm. Broadening of the 49 nm peak suggests non-uniformity in the strain profile due to lateral strain relaxation. (right) Average transverse strain obtained from the Raman peak shift Δω (7) relative to unstrained Ge (solid symbols), and from the simulations shown in Fig. 3 (open symbols). The measurements are consistent with the simulations.

- Bond and etchback to form SGDOI wafers
- Hybrid lithography: EBL to form NWs and PL for S/D pads
- Pre-ald clean: NH4OH:DI
- High-K/Metal-Gate ALD: O3 surface passivation, 40Å HfO2, WN deposition
- Gate RIE and S/D implant (B, 5keV, 2×10^{15})
- LTO ILD deposition and S/D activation at 500˚C for 30 minutes
- Contact via open, Ti/Al metallization and FGA at 450˚C for 30 minutes

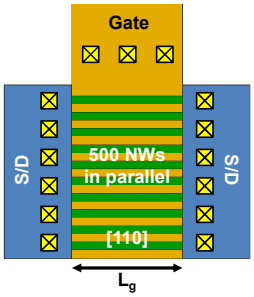

Fig. 6: (left) Process flow used to fabricate s-Si/s-Ge trigate nanowire p-MOSFETs with high-κ/metal gate. (right) Top-down schematic of the mobility-extraction device.

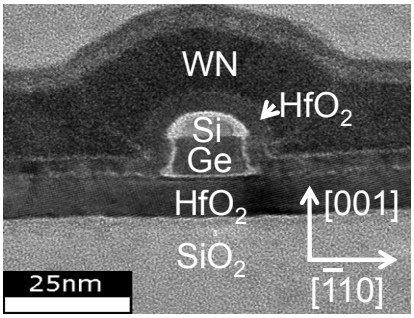

Fig. 7: XTEM of a nanowire with W_{NW}=18nm. The channel direction (into the page) is [110]. The quoted NW widths in this work were measured by plan-view SEM using images taken during processing.

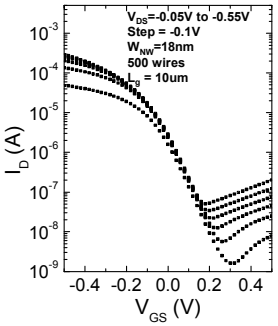

Fig. 8: Transfer characteristics for W_{NW}=18 nm, L_g=10 µm. The device has SS~85 mV/dec. and $I_{max}/I_{min}>10^4$ for V_{DS}= -50 mV.

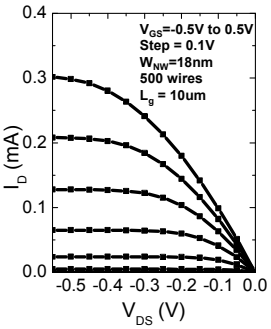

Fig. 9: Output characteristics for a device with W_{NW}=18nm, L_g=10µm and 500 wires in parallel.

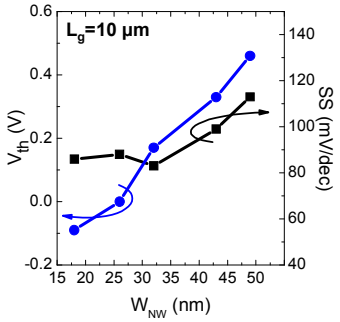

Fig. 10: V_{th} and SS vs. W_{NW}. V_{th} was extracted from the Y-function method(8). V_{th} shift as a function of W_{NW} may be caused by backside/sidewall D_{it}. The planar (biaxial) device has SS and V_{th} of 205mV/dec. and 0.8V, likely influenced by backside D_{it}.

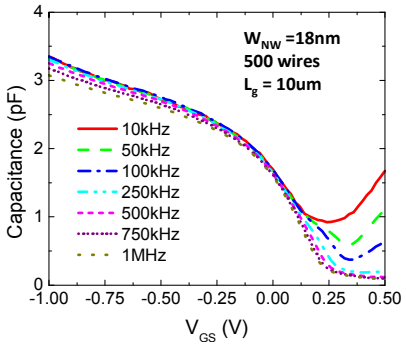

Fig. 11: Split C-V for W_{NW}=18 nm, L_g=10 µm and 500 wires. Little frequency dispersion is observed in inversion. A frequency of 500 kHz was used for accurate mobility extraction.

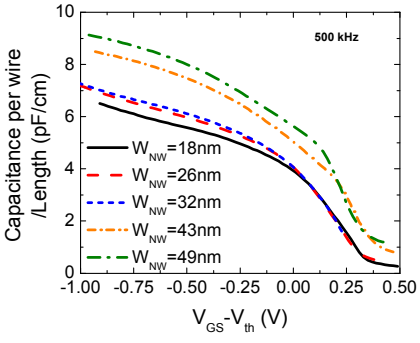

Fig. 12: Measured capacitance per wire per unit length for W_{NW}=18, 26, 32, 43 and 49nm. This data was used for mobility extraction.

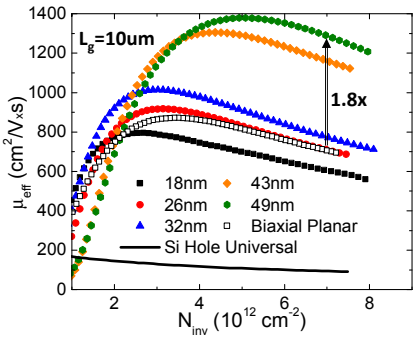

Fig. 13: Effective hole mobility for trigate and on-chip planar (biaxially strained Ge) FETs and Si hole universal (9). N_{inv} for trigates is calculated using a conservative W_{eff}=500•(W_{NW}+2H_{NW}). The mobility of the planar FET was extracted using W=L_g=100µm. The mobility for W_{NW}=49nm is ~ 1.8x the biaxial strained Ge mobility at N_{inv} =7x10^{12} cm^{-2}.

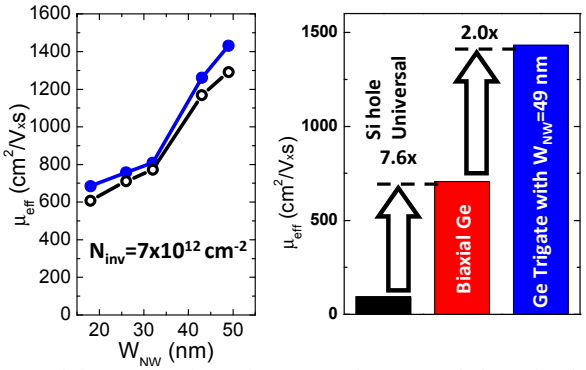

Fig. 14: (left) A comparison of as-extracted (open symbols) and series resistance corrected mobilities (closed symbols) at N_{inv} =7x10^{12} cm^{-2} for different W_{NW}. The correction increases the mobility by ~ 10%. The series resistance (~1500 Ω-µm) was extracted from L_g=1 µm devices by plotting R_{total} vs. 1/(V_{GS}-V_{th}-V_{DS}/2) and linearly extrapolating to 1/(V_{GS}-V_{th}-V_{DS}/2)=0. (right) Mobility comparison at N_{inv} =7x10^{12} cm^{-2}.

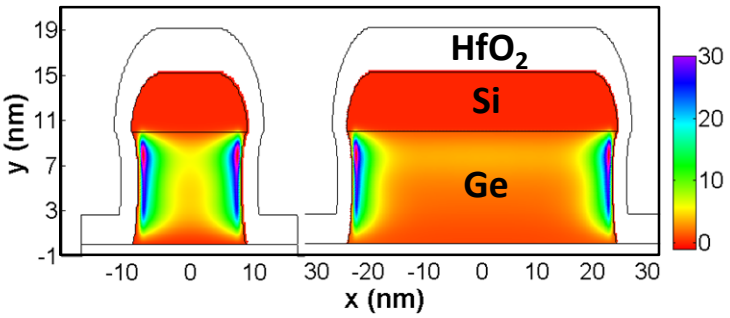

Fig. 15: Simulated hole densities (nextnano^3) for W_{NW}=18 and 49nm at V_{th}-V_{GS} ≈0.2 V, using a 6×6 k.p method; the scale has units of 10^{18} cm^{-3}. The impact of strain on the energy bands was taken into account. The sidewall EOT (~1 nm) is smaller than the top EOT (~1.5 nm) due to differences in the GeO_x and SiO_x interface layers (2,10). A large fraction of the carriers are located near the sidewalls because of this and the s-Si/s-Ge valence band offset. The sidewalls are also the regions with the most asymmetric (approaching "uniaxial") strain (Fig. 3).

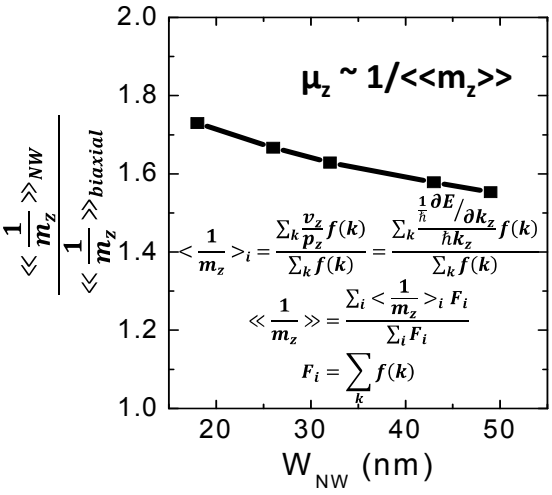

Fig. 16: Simulated enhancement in average inverse effective mass in the transport direction, <<1/m_z>> for nanowires relative to planar biaxial strained Ge. The simulation shows a large increase in inverse effective mass (~1.6×) for asymmetrically strained nanowires relative to the biaxial case, consistent with the measured mobilities for wide trigates. The average inverse effective mass for the *i*th eigenstate (<1/m_z>$_i$) is the inverse transport effective mass for all k-vectors weighted by the occupancy at each k-vector. The average inverse transport effective mass (<<1/m_z>>) is calculated by the sum of <1/m_z>$_i$ multiplied by the fraction of holes present in each eigenstate for all 80 eigenstates used in the simulations.

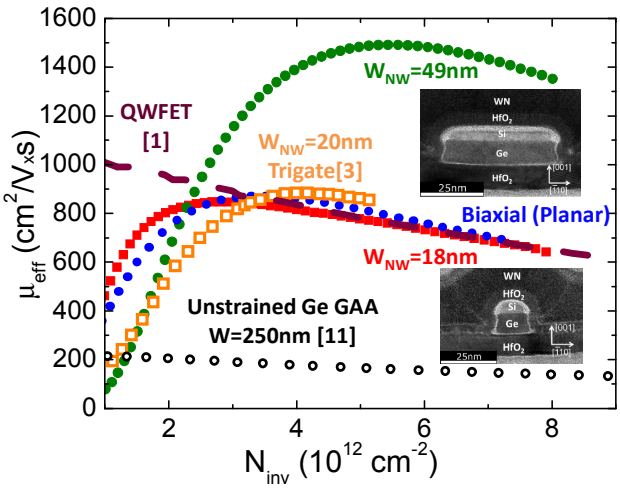

Fig. 17: Series resistance corrected mobilities (solid symbols) for trigates with W_{NW}=18 and 49 nm vs. previously published results for non-planar and state-of-the-art planar strained Ge FETs with high-k dielectrics. Insets show TEM of NW cross-sections for this work. Biaxially strained and W_{NW}=18nm from this work have mobilities comparable to state-of art strained Ge devices. The W_{NW}=49 nm device shows dramatically improved transport relative to the highest reported strained Ge mobilities.