Optimization of the Electron Hole Bilayer Tunneling Field Effect Transistor

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In order to reduce the power consumption of modern electronics, the operating voltage needs to be significantly reduced. The electron hole bilayer tunneling field effect transistor (bilayer TFET) has the potential for reduced voltage operation. [1, 2] The device structure is shown in Fig. 1. Recent simulations of the bilayer TFET show poor on-state current [1] and electrostatic gate efficiency [2]. In this work we propose a new biasing scheme to improve gate efficiency by exploiting quantum capacitance and create a new model to analyze the tradeoff between gate efficiency and on-state current to find the optimal device design.

The band diagram and circuit model for the device is shown in Fig 2. In order to maximize the gate efficiency (dE_{OL}/dV_{G1}) we want to maximize the change of the energy overlap E_{OL} (shown in Fig 2a) with respect to the gate voltage V_{G1} while all the other voltages are held constant. This means that we want to maximize dV_1/dV_{G1} while minimizing dV_2/dV_{G1}. Consequently, we want the body as thick as possible to isolate V_2 from V_{G1}. Additionally, we want to minimize the electron quantum capacitance by minimizing the electron density while maximizing the hole quantum capacitance by increasing the hole density until the p-side is degenerate. Unfortunately, the carrier density and body thickness are constrained by the required on-state conductivity. The fewer electrons present in the channel, the lower the channel conductivity and the thicker the body, the lower the tunneling probability. Thus, we optimize these tradeoffs to maximize the device performance.

According to the ITRS, we need an on-state conductivity around 1 mS/μm in order to be competitive with current CMOS logic. The subthreshold slope will be determined by the abruptness of the band edges and the gate efficiency. Ideally, no current will flow until the confined electron and hole states overlap when E_{OL} equals zero, resulting in an infinitely steep subthreshold slope. In practice, there are states below the band edge which result in a finite subthreshold slope.

We analyze the device using 1) a ballistic MOSFET model to determine the required charge density, 2) the circuit model in Fig 2(b) to determine the potentials and gate efficiency, and 3) a WKB based 2d-2d tunneling current model [3] to determine the conductance. The key design parameters are the thickness of the bilayer body, t_{Body}, the length of the channel L_C, the channel material (silicon, germanium or InAs), and the gate workfunctions.

In Fig 3(b) we plot the body thickness required for an on-state conductivity of 1 mS/μm for different channel lengths. As expected, InAs can tolerate much thicker bodies as the band gap and effective mass are lower. To compare the different materials we consider a 10 nm long channel in the rest of the discussion. To achieve the desired on-state conductivity, Si, Ge and InAs need to be 4.7 nm, 11.4 nm and 15 nm thick, respectively. The required tunneling probability is shown in Fig 3(a). Interestingly, it should be possible to achieve an on-state conductivity of 1 mS/μm in Si if the body is sufficiently thin. However, that requires an electric field around 4.9 MV/cm, tunneling barrier thickness of 2.2 nm and tunnel probability of 3×10^{-4}. While the tunneling model used was calibrated to experimental data at lower fields, there is currently no measurement of what will happen at that such high fields.

Fig 4 shows that the gate efficiency is almost the same for all three materials at the optimal body thickness and is around 43% for a 10 nm channel. Even though silicon has a superior gate efficiency at a given body thickness [2], once we optimize the thickness for a given on-state, the different materials are almost the same.

While all three materials have the same on-state and gate efficiency by modifying body thickness, the DC bias or gate workfunctions required will be drastically different between the materials. Fig 5 shows the DC bias required to align the energy eigenstates. For a 10 nm channel, the voltage across both gates will be 5 V, 2.3 V and 1.4 V for Si, Ge and InAs respectively. It may be possible to achieve the DC bias required for InAs through work functions, but it will be very difficult to achieve the 2 or more volts that is required for Silicon and Germanium. Furthermore, the high electric field required in silicon will cause the gate oxide to break down.

We found that a 15 nm thick InAs bilayer represents the best tradeoff between gate efficiency, on-state conductivity and required gate workfunctions. We also found that an 11 nm thick germanium bilayer could be interesting if the gate workfunctions could be sufficiently engineered.

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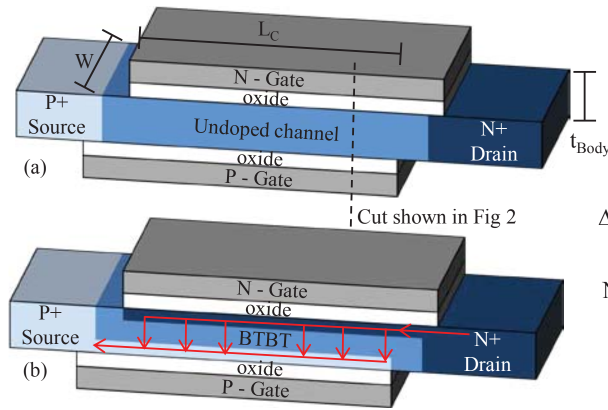

Fig 1: (a) Electron-hole bilayer TFET structure (b) Structure with the current path and inversion layers.

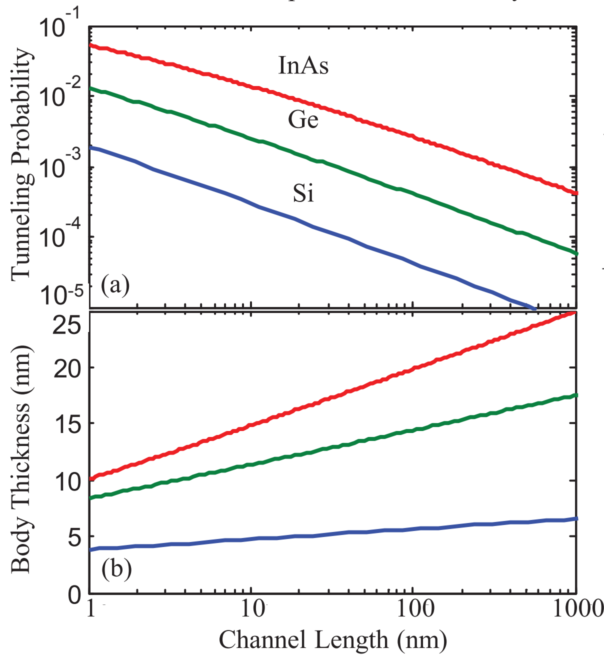

Fig 3: The required tunneling probability (a) and body thickness (b) for a 1 mS/µm conductivity are plotted. The required tunneling probability depends on the density of states and the confined energy.

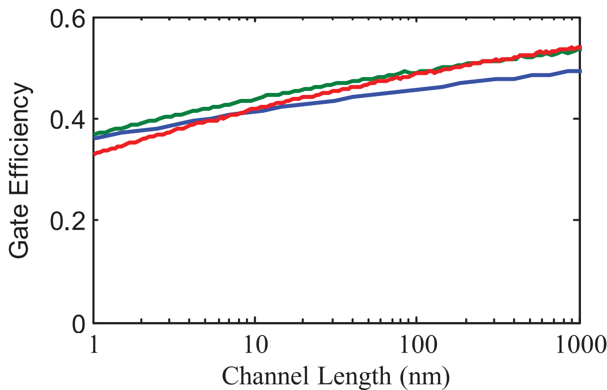

Fig 4: The gate efficiency averaged over a 100 meV change in E_{OL} for all three materials is similar.

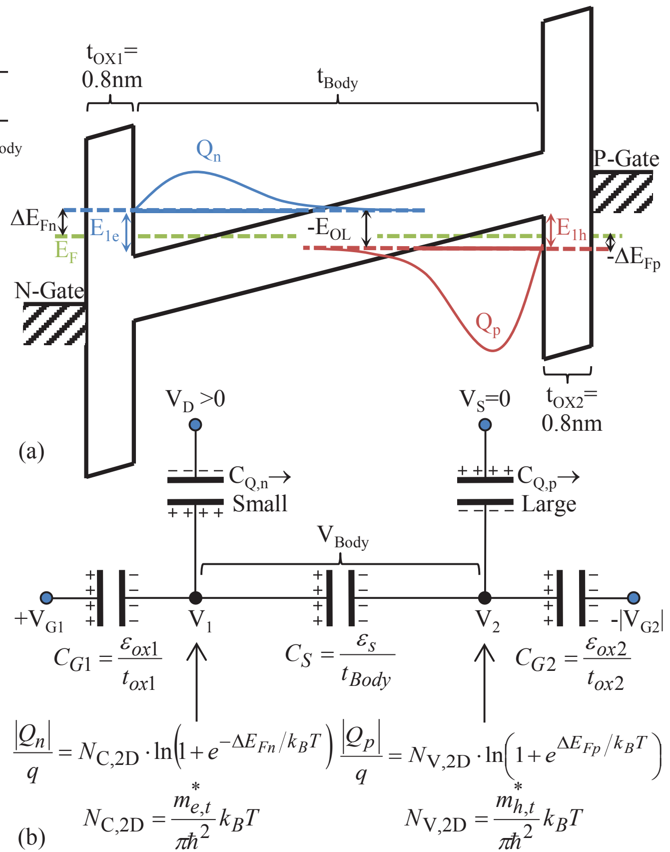

Fig 2: (a) Vertical band diagram with quantum ground states shown (b) Equivalent circuit model of the device

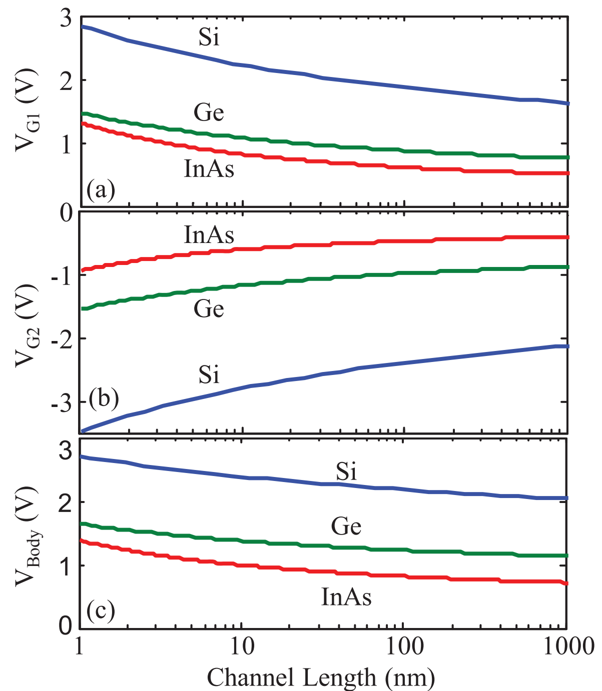

Fig 5: The top gate (a) and back gate (b) voltages required to align the eigenstates is plotted. The voltage across the body (c) at eigenstate alignment is also plotted.