InAs/GaSb QW Tunneling Project: Status, Results, & Direction

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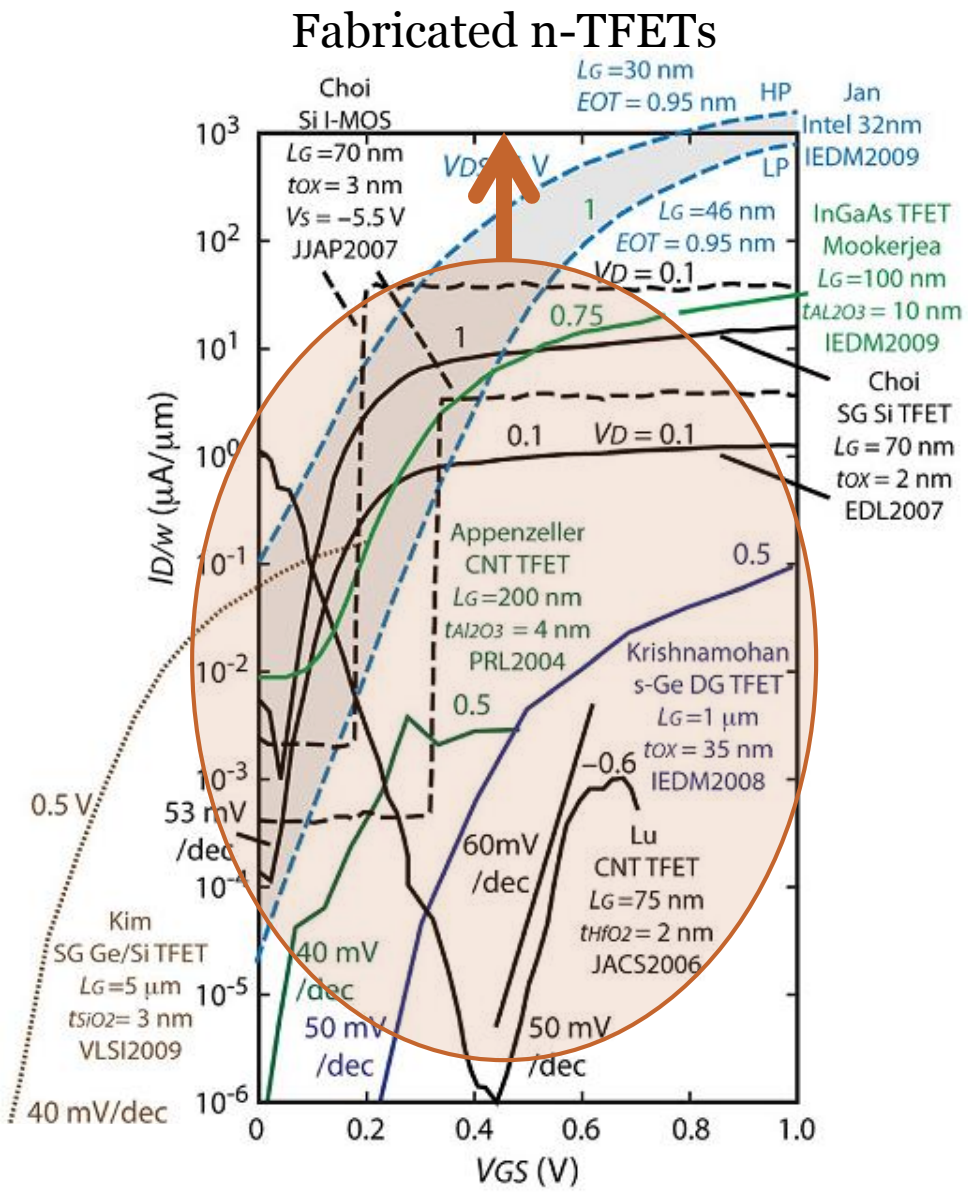
Dimitri Antoniadis, MIT
Jamie Teherani, MIT
Judy Hoyt, MIT
Mathieu Luisier, Purdue/ETH Zurich

Massachusetts Institute of Technology

Previous TFET Results

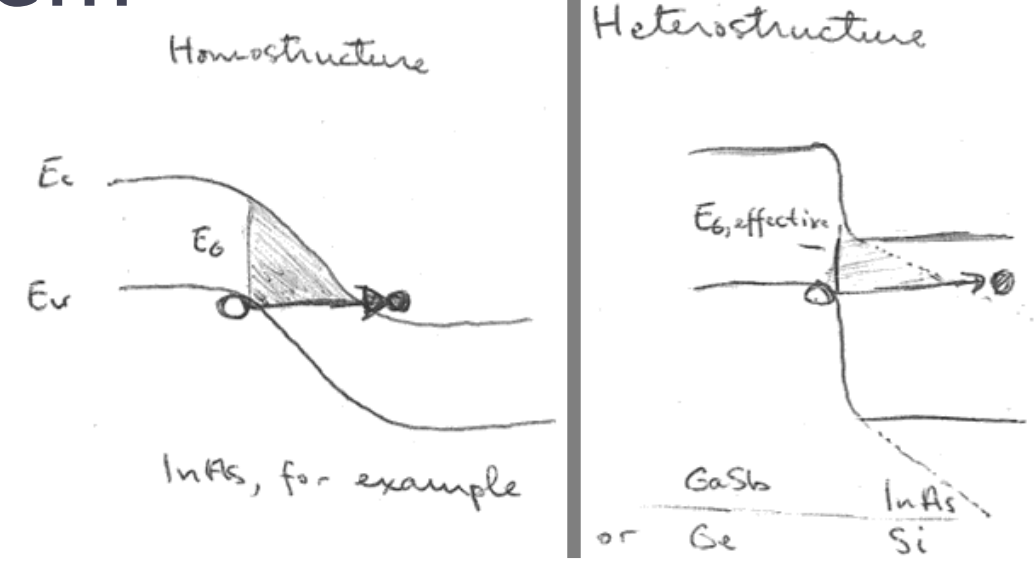


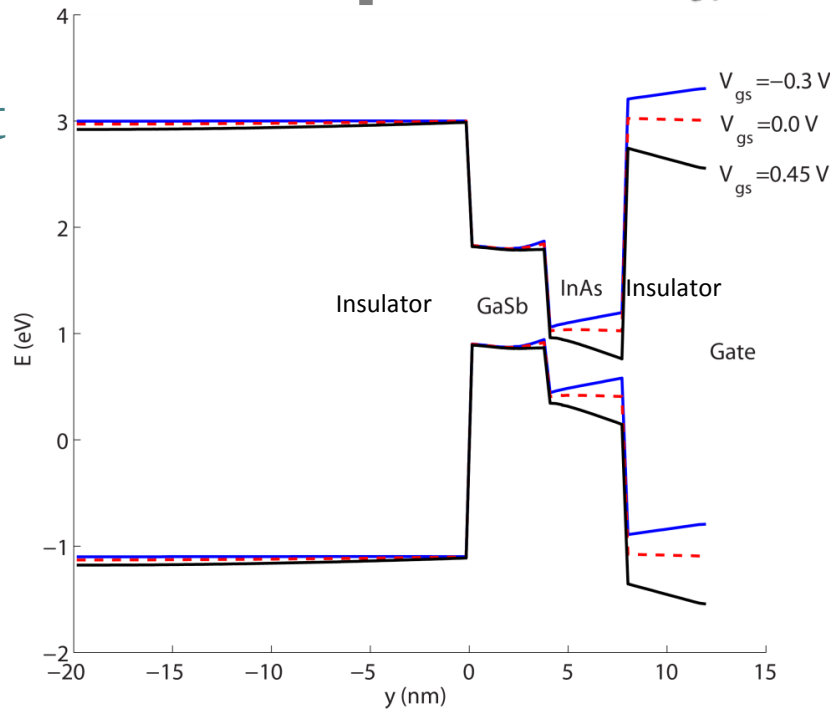
- Though SS < 60 mV/dec has been seen in some fabricated devices, current levels are very low
- Tunable variables
  - Material system
    - Homostructure/hetero
    - Direct/indirect band gap
  - Structure
    - Lateral/vertical/pocket
    - 3D/2D/1D

A. C. Seabaugh and Qin Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095-2110, 2010.

New Material System

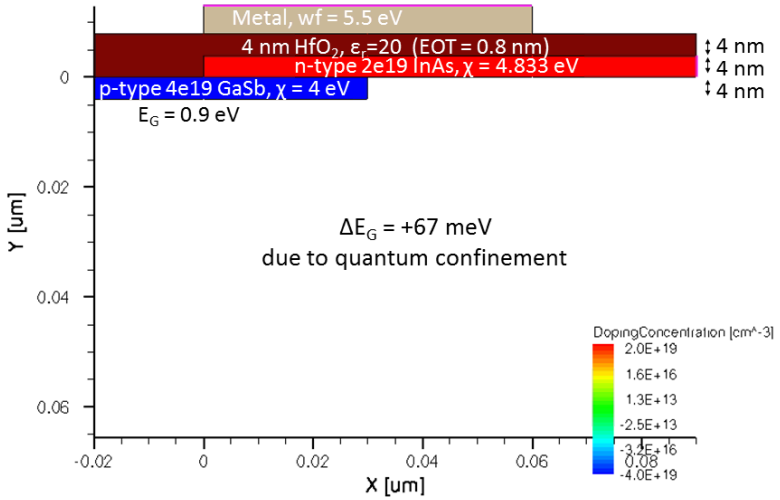
- Homostructure → Heterostructure
  - To significantly reduce tunnel barrier (E_G or $E_{G,effective}$)
- Indirect → Direct
  - No (efficient) Si diodes/lasers
  - Indirect processes too inefficient
- InAs/GaSb
  - Direct gap
  - Heterostructure gives $E_{G,effective}$ ~ 0 eV
  - Small tunneling barrier
  - Lattice mismatch < 0.7%



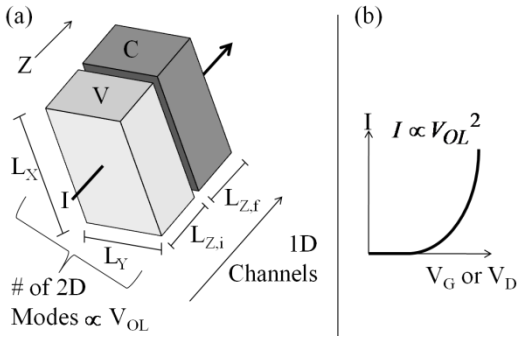


New QW Vertical Structure

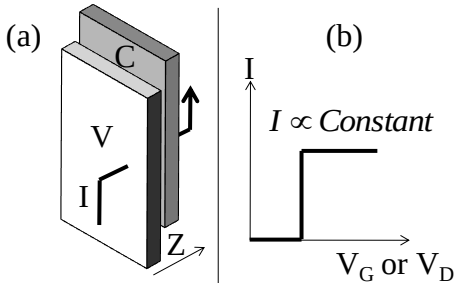
- Electrostatic benefits
  - Tunneling in the direction of the applied gate field
  - Possibility for areal tunneling
  - Good control over InAs surface potential
- Density of States
  - 2D to 2D tunneling could have a “step-like” turn-on



3D to 3D



2D to 2D



Sapan Agarwal, 2010

New Simulation Platform

Physical Models

- 3D Quantum Transport
- Effective Mass and Full-Band
- Atomistic Representation
- Ballistic and Dissipative
- Out-of-Equilibrium

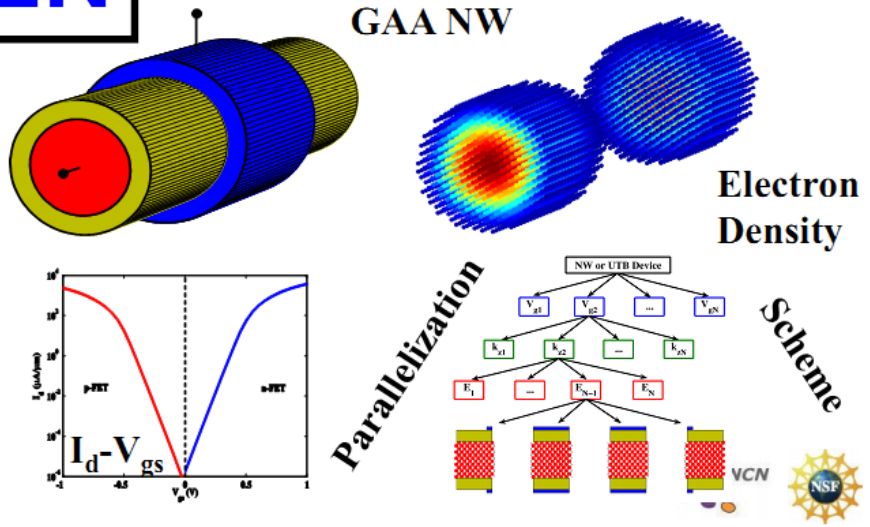
Device Engineering

- Output Characteristics
- Short-Channel Effect, DIBL, SS, Gate Leakage, Strain, …
- Internal Data: Current Flow, Charge, Electrostatics

OMEN

- C++ Implementation
- High Performance Numerical Libraries (Blas, Lapack, …)
- Quad-Level Parallelization (MPI and OpenMP)

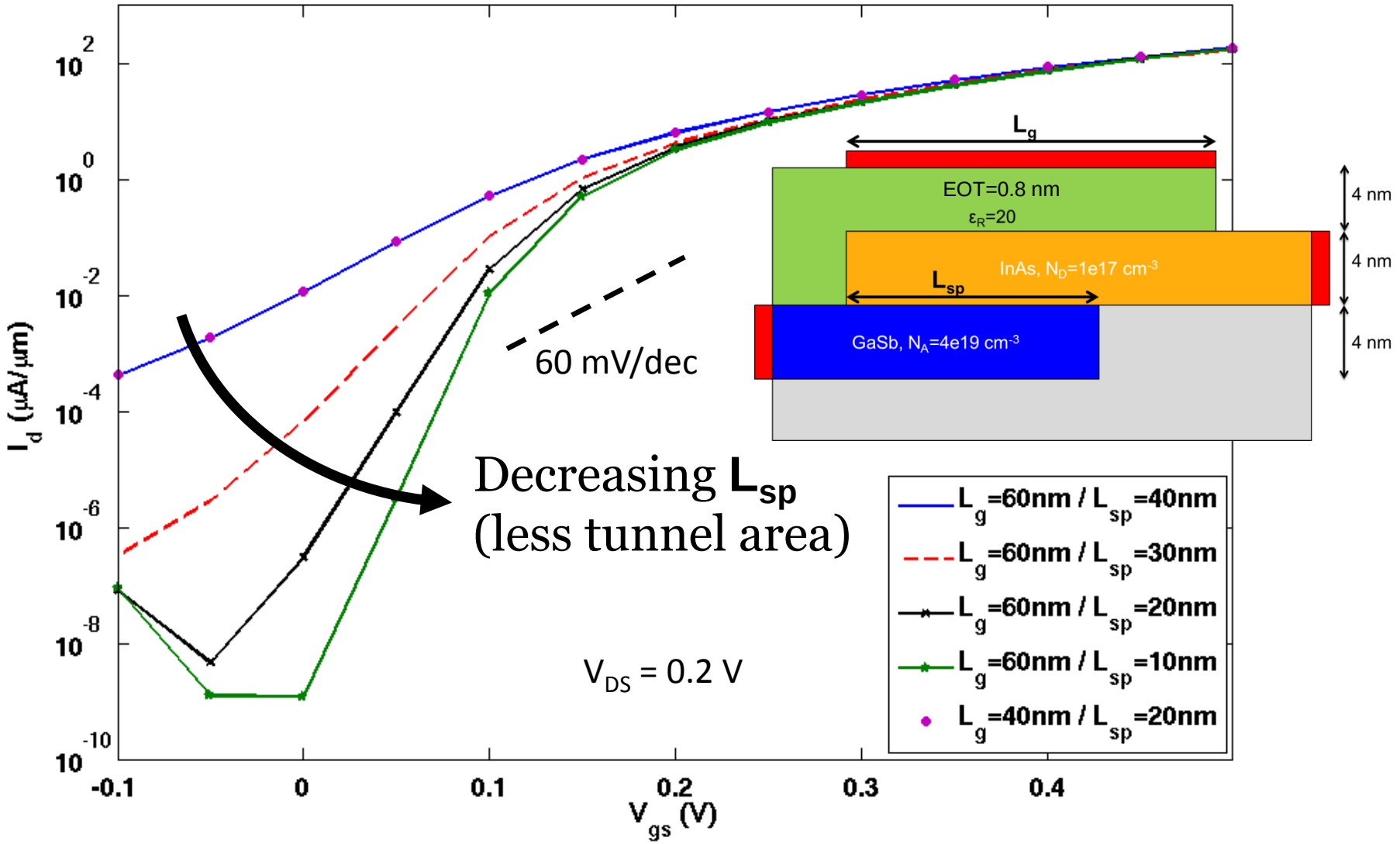
Numerical Implementation



~100,000 CPU hours/simulation

From M. Luisier et al., "Design Study of III-V HEMTs and TFETs using OMEN, a Novel Quantum Transport Simulator," Nov. 2009.

OMEN Simulation Results



- Off-current is reduced as source is further separated from drain
- Need to better understand the tunneling in order to optimize the device structure

Sdevice Simulation Platform

- Classical simulator
- Single conduction band and valence band
- Assumes parabolic bands
- Isotropic, constant effective mass
- BTBT model based on WKB approximation

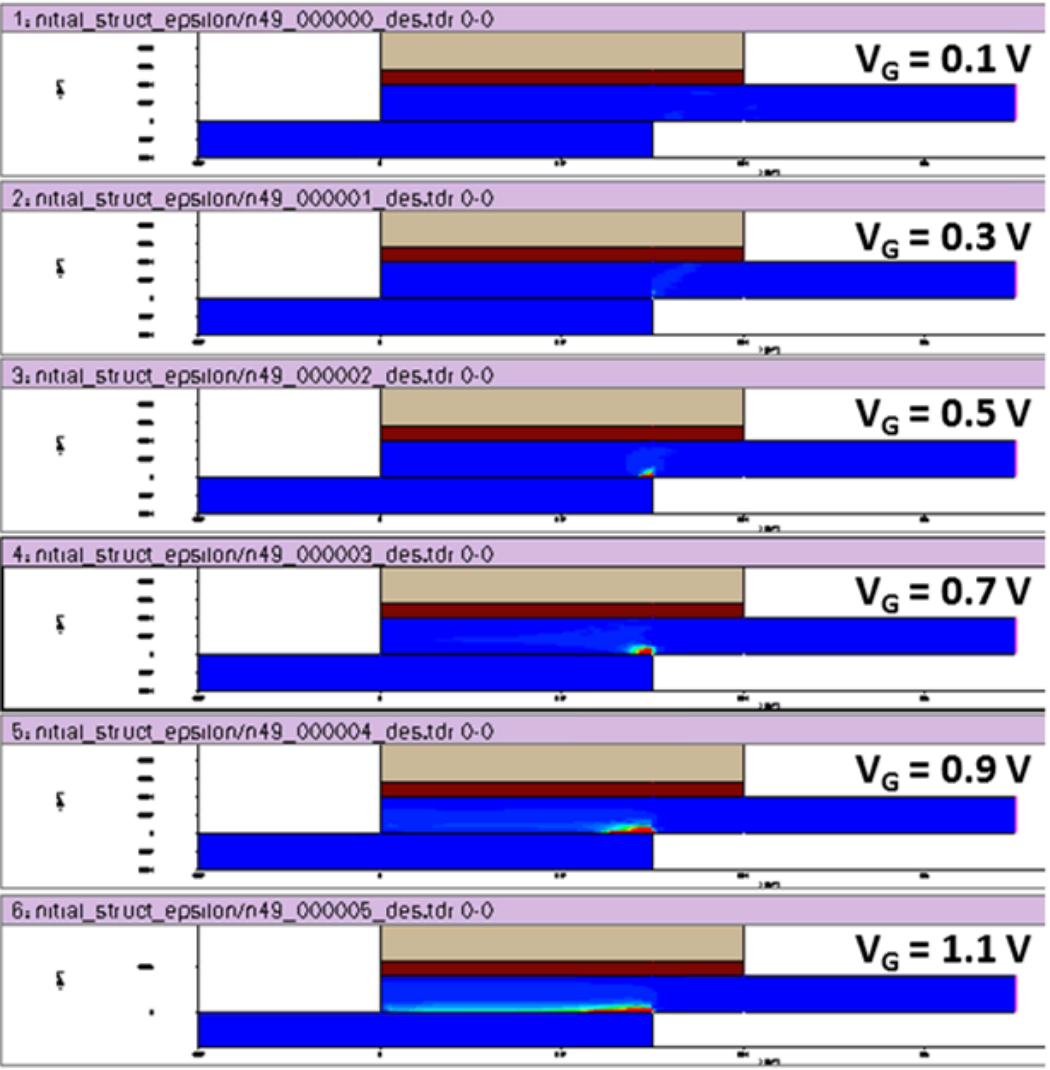
$$R_{\text{net}} = A\left(\frac{F}{F_0}\right)^{P} \exp\left(-\frac{B}{F}\right)$$

~0.25 CPU hours/simulation

Non-areal Scaling

Electron Generation ($cm^{-3}s^{-1}$)

Linear Scale



The majority of tunneling only occurs in a small region in the InAs layer.

Scale:
Blue 0
Red 1e29

Scale:
Blue 0
Red 1e29

Scale:
Blue 0
Red 2e29

Scale:
Blue 0
Red 4e29

Further optimization of the structure required?

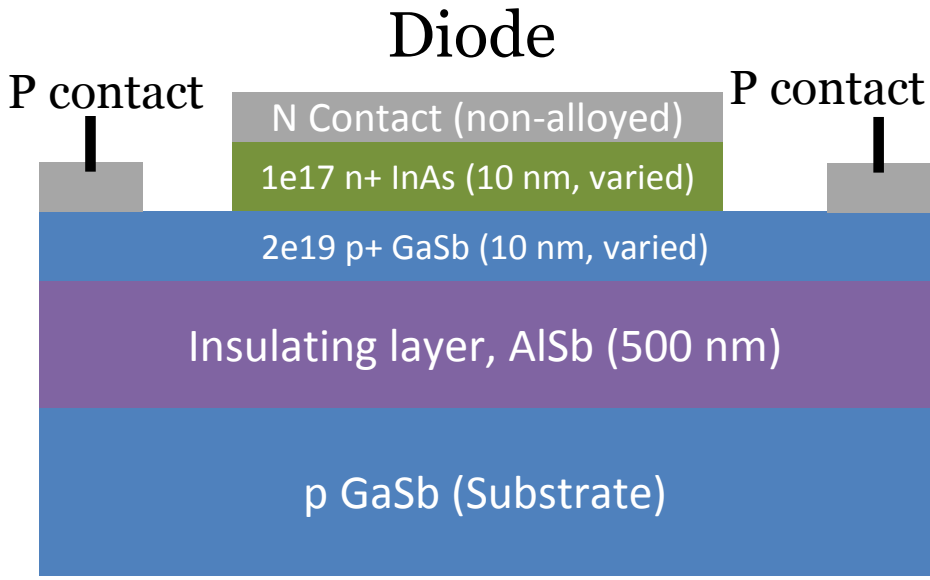
Or ideal for scaled device geometry?

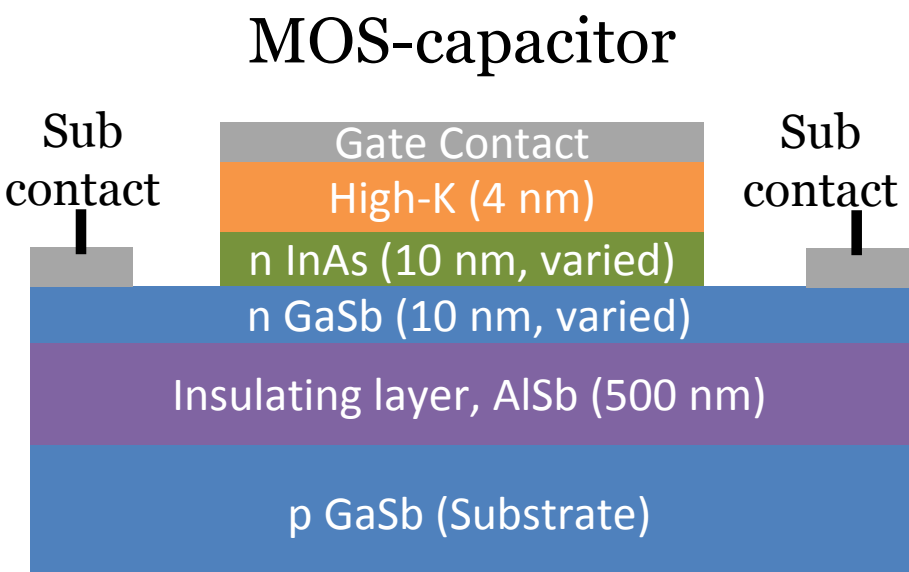
V_{DS} = 0.2 V

Current Experimental Work

- Begin with 2-terminal structures
  - Diodes
    - Gauge maximum tunneling current
    - Analyze 2D to 2D tunneling
    - “Fabricatablity”
  - MOS-capacitors
    - Extract material parameters
    - Characterize high-K/III-V interface

Material provided by Brian Bennett, NRL





Goals of Current/Future Work

- Electronic characterization of InAs/GaSb
- QW properties
  - Subband energies
  - Varied InAs and GaSb thicknesses
- “Calibration” of fast device simulator to advanced simulator (Sdevice to OMEN)
  - Simulators used in tandem to verify/identify interesting features
- Further optimization of structure